Application Report
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NanoStar ™ & NanoFree ™ 300μm Solder Bump Wafer Chip-Scale Package Application

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ABSTRACT

The NanoStar™ Wafer Chip-Scale Package (WCSP) is a family of bare die packages developed for applications that require the smallest possible package. WCSP provides electrical interconnection via solder spheres attached to the die and is aligned with JEDEC package standard MO−211[1]. NanoStar, with advanced materials engineering technology, has demonstrated excellent board level reliability that allows it to be used without the need for underfill adhesives, unlike conventional solder-bumped Flip Chip devices. This advanced design allows standard, low-cost surface-mount technology (SMT) assembly processes to be used successfully. This application guide provides the necessary design and reliability information to apply the NanoStar 300μm solder bump packages.

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1 Introduction

In today's mobile environment, there seems to be an insatiable market demand for the smallest and lightest possible electronic products with high reliability. Electronics manufacturers are designing smaller and smaller products with each generation and release. Many different types of packages have been developed to meet this need. Popular package sizes such as MSOP, SOT−23, SC−70, and QFN outlines are quite large in comparison to a die size or wafer-level chip-scale package. (See Figure 1.) There are several names for die size packages, including Flip Chip (FC), Wafer-Level Chip Scale Package (WLCSP), and Wafer Scale Package (WSP). Regardless of the package name, however, the benefits to a die size package are clear: the smallest possible form factor for an integrated circuit silicon die is the die itself.

TI utilizes new advanced polymer technology materials to enhance the board-level reliability of the NanoStar™ 300µm solder ball packages. Many suppliers of WCSP packages use relatively brittle re-passivation polymeric materials. While these brittle materials work well for some applications, they have been shown to have poorer performance for 300µm solder sphere-bumped devices.[2] As a result of the new polymer technology available in the NanoStar package, TI customers do not have to experience premature device or reliability failures caused by brittle re-passivation and often seen in competitive parts.

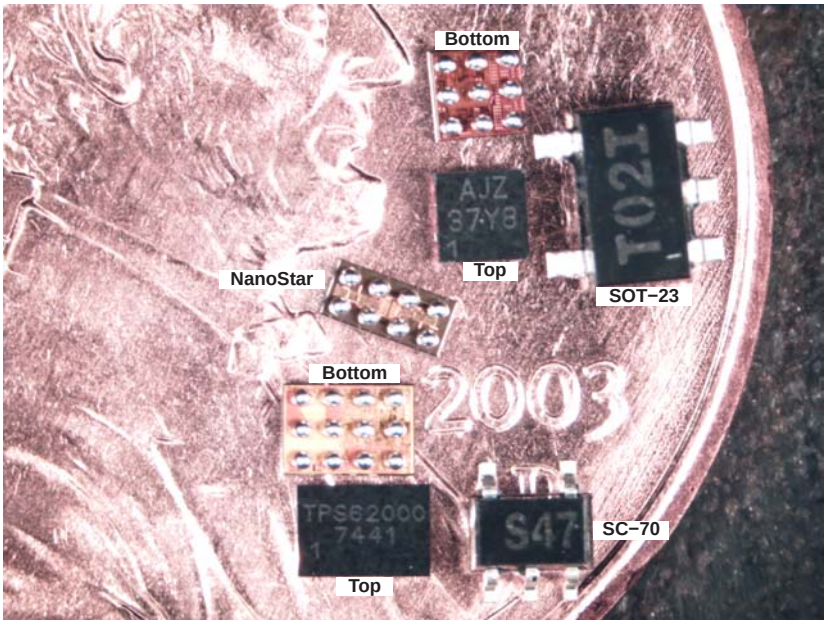


Figure 1. NanoStar™ WCSP, SOT−23, & SC−70 Size Comparison

There are many challenges in interconnecting the micron-level world of silicon to enable bare die use in the millimeter-based world of SMT assembly. The proper system design for a die size package application is critical. NanoStar WCSP has been developed in 4−36 pin packages to enable high performance products to be as small as possible. A summary of the available packages is provided in Section 1.1. This package size not only enables smaller products, but also provides improved electrical performance. The performance increase is a direct result of shorter interconnections and, consequently, reduced parasitic losses due to interconnect length.

NanoStar WCSP adds other visible features, as well. All NanoStar devices are laser-marked to provide device identification and production lot tracking. Most analog NanoStar devices also have a protective backside surface coating to improve performance. This opaque coating reduces the parametric shifts that can occur due to the light sensitivity of IC structures. The coating allows a WCSP to provide the same level of consistent performance obtained from a molded package device.

This application note provides the necessary information to apply NanoStar technology with maximum success. The enclosed mechanical, electrical, and thermal package information, in addition to printed circuit board (PCB) design recommendations and reliability data, are the culmination of another enabling technology developed for Texas Instruments' customers.

1.1 Package Offerings and Nomenclature

Table 1 shows the initial NanoStar WCSP package family lineup. As customer demand increases and more devices use the TI WCSP, this list is expected to grow. Please visit the TI web site for the latest list of products that use the NanoStar package family.

While the NanoStar name covers this entire WCSP family, TI also uses the NanoFree™ term to differentiate devices that are available in lead-free solder alloys. For ease of reading, this document applies to both versions, and will typically use only the NanoStar name. Where differences are noted for lead-free packages, the NanoFree name will be specifically inserted.

Table 1. NanoStar™ & NanoFree™ 300μm Solder Bump Package Family Summary(1)

Package Designator(2)	Minimum "D"	Maximum "D"	Minimum "E"	Maximum "E"	Array Pinout
YEB, YZB	0.85	1.65	0.85	1.65	4
YEC, YZC	1.35	2.15	0.85	1.65	6
YED, YZD	1.85	2.65	0.85	1.65	8
YEF, YZF	1.35	2.15	1.35	2.15	9
YEG, YZG	1.85	2.65	1.35	2.15	12
YEH, YZH	1.85	2.65	1.85	2.65	16
YEJ, YZJ	2.35	3.15	1.85	2.65	20
YEK, YZK	2.35	3.15	2.35	3.15	25
YEL, YZL	2.35	3.65	2.35	3.15	30
YEM, YZM	2.85	3.65	2.85	3.65	36
YEU, YZU(3)	0.95	1.45	1.25	1.75	5

NOTE 1: Package availability varies based on currently released products. Some of the above packages may not be available. Please reference the TI web site (www.ti.com) for released packages.
NOTE 2: A **Z** designator indicates NanoFree devices.
NOTE 3: Staggered array device.

The NanoStar WCSP packages in this report are referred to as simply NanoStar or WCSP packages. The NanoStar 300μm package family currently encompasses the three-letter TI package designators YEB, YEC, YED, YEF, YEG, YEH, YEJ, YEK, YEL, YEM and YEU for tin-lead solder bumped devices. NanoFree™ Lead-Free solder bumped devices will use the package designators YZB, YZC, YZD, YZF, YZG, YZH, YZJ, YZK, YZL, YZM and YZU. The lead-free WCSP packages are the exact same dimensions as the lead-containing counterparts.

2 Physical Description

2.1 Package Characteristics

The NanoStar package family is a Die Size BGA as identified by the JEDEC standards organization [3]. Simplistically, the package is the silicon die with solder interconnects located on the active surface, and identification marking on the die backside. (See Figure 2.) These solder interconnects are placed on the PCB through conventional SMT processes to form a working circuit. TI has developed two different construction technologies to enable broad use of the WCSP in a variety of applications. These two approaches are called *Direct Bump* (or *Bump-On-Pad* [BOP]) and *Re-Distribution Layer* (RDL) technology.

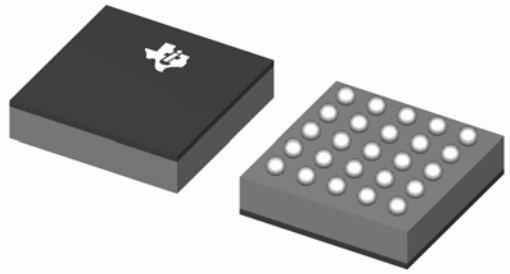


Figure 2. NanoStar WCSP

The TI Direct Bump technology is used on devices designed specifically to use WCSP. The solder bump is placed directly on the device bond pad that is normally reserved for the wire bonding process in conventional packaging. A cross-sectional view of direct bump construction is given in Figure 3. The construction consists of:

- A protective polymer re-passivation layer (to cover the delicate silicon surface)
- Under-bump metal (UBM) contact
- 300µm solder sphere

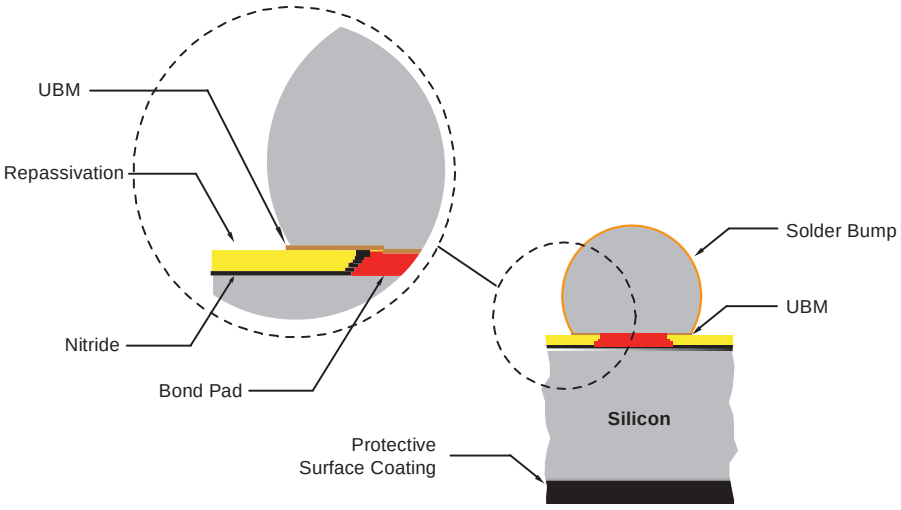


Figure 3. Direct Bump WCSP Construction Cross-Section

Texas Instruments' RDL technology can be used on devices designed for WCSP as well as other package types. This method allows introduction of a broader portfolio of devices that may not have the production volume to justify the tooling costs of a brand new device. Using RDL technology, the solder bump is placed on a bond pad specially created in a different location than the bond pad originally designed for the wire bonding process.

A cross-sectional view of a typical RDL application is given in Figure 4. RDL construction consists of:

- A protective polymer re-passivation layer (to cover the delicate silicon surface)
- A copper metal layer to move the interconnect to the proper array location
- A second polymer layer to insulate the RDL layer
- Under-bump metal (UBM) contact
- 300µm solder sphere

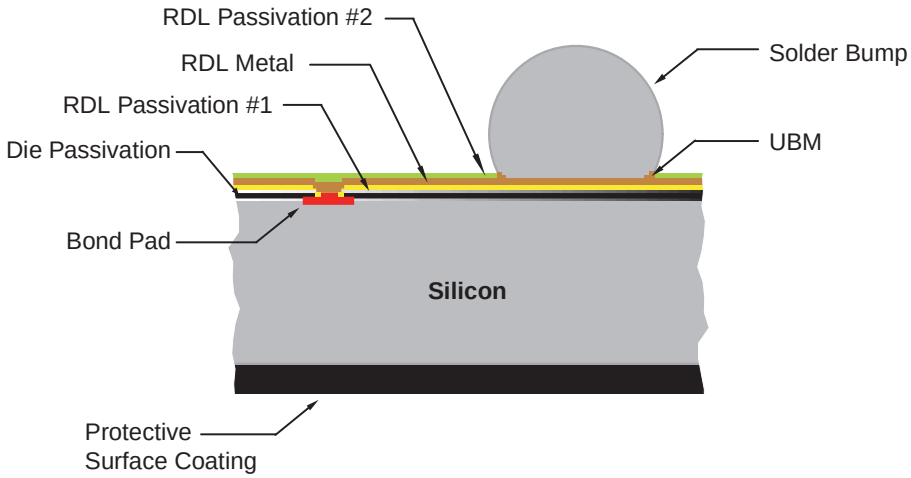
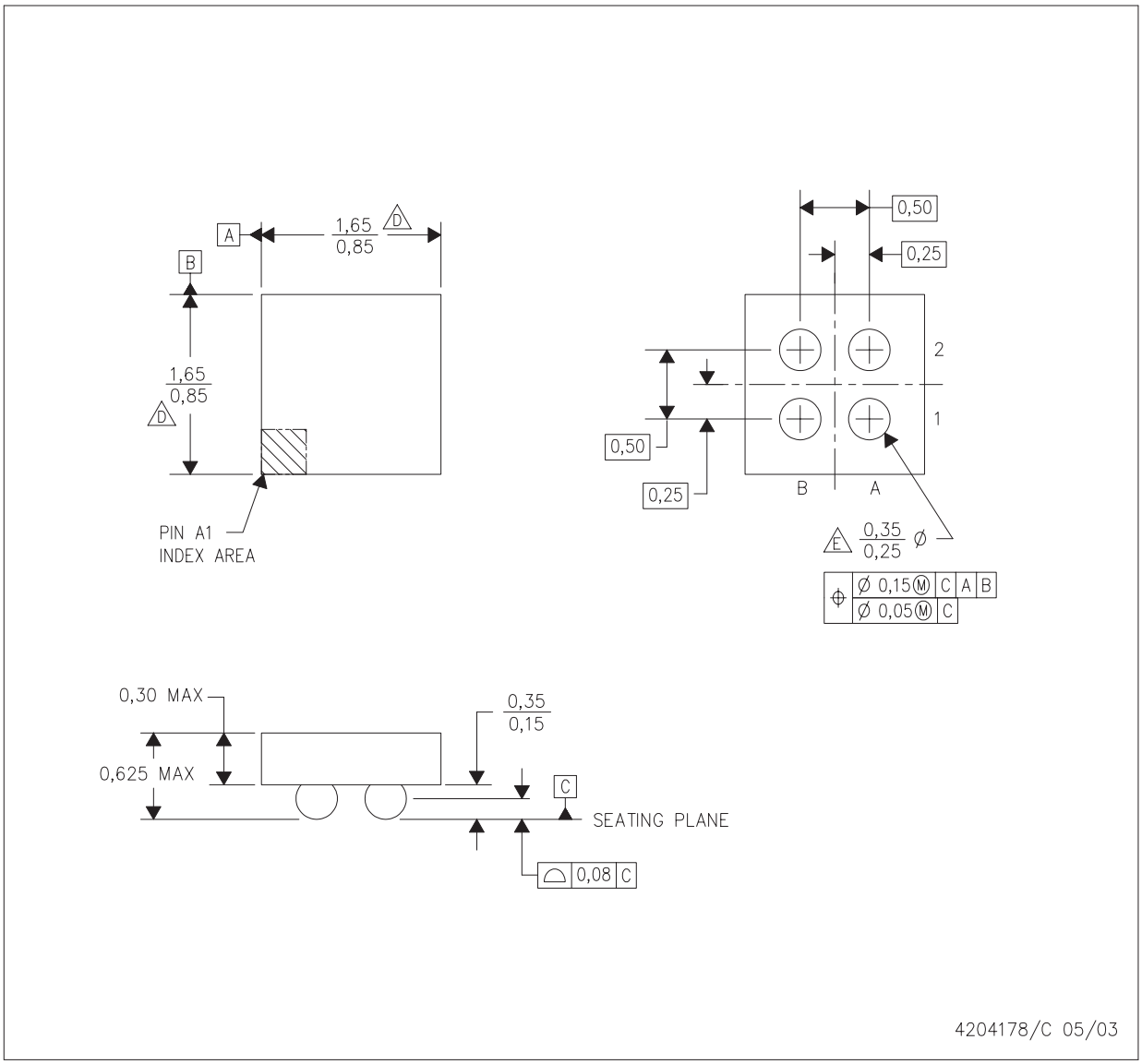


Figure 4. RDL WCSP Construction Cross-Section

2.2 NanoStar Package Dimensions

Typical NanoStar package dimensions are shown in Figure 5. Current released package drawings are available through the TI web site (www.ti.com). These package drawings are generic for each array footprint. The drawings provide details of solder bump tolerances, package thickness, and basic size information. Keep in mind that NanoStar is a die size package; therefore, the exact package outline varies within a given package footprint. Each device in the NanoStar package will detail the exact product device size in the relevant data sheet.

YEB (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Die size package configuration.
D. Reference Product Data Sheet for die size and orientation.
E. Reference Product Data Sheet for array population.
2 x 2 matrix pattern is shown for illustration only.
F. This package is Tin–Lead (SnPb).
Refer to YZB (Drawing #4205055) for Lead Free version.

Figure 5. YEB Package Dimensions

2.3 Thermal Performance

Typical thermal performance of the NanoStar devices can be found in Table 2. Due to the small size, low profile, and location of the power plane, the primary path for heat dissipation in the NanoStar device is through the board. This makes the Theta JB a more significant number than Theta JA when considering the thermal characteristics of a NanoStar package. (Theta JA, or θ_{JA}, is junction-to-air; Theta JB, or θ_{JB}, is junction-to-board). Thermal performance can be improved for all package sizes by using thermal planes in a multilayer PCB under the NanoStar device. It is not recommended to clamp any heatsink to the top of a NanoStar device. Figure 6 shows a graphical comparison of the thermal resistance change across a range of package designators for a simple JEDEC 1S0P board. Figure 7 shows the possible improvement by using a typical four-layer JEDEC 2S2P board.

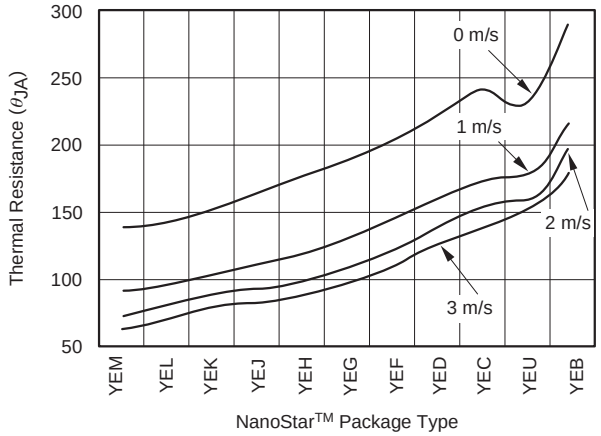


Figure 6. JEDEC 1S0P Thermal Performance Data Graph

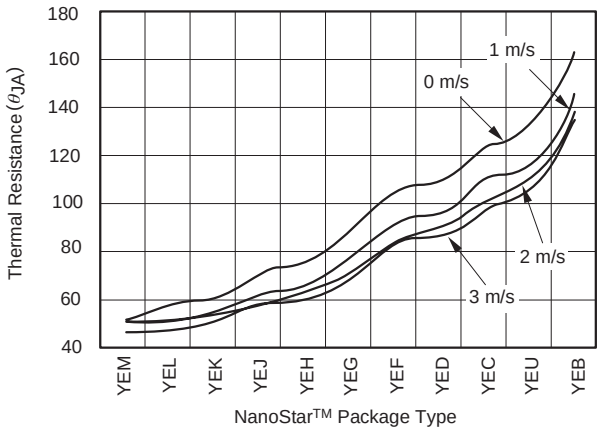


Figure 7. JEDEC 2S2P Thermal Performance Data Graph

Table 2. Simulated Thermal Resistance Data(1)

Chip Size (mm)	Linear Airflow Velocity (m/s)					
	(°C/W)	0 m/s	1 m/s	2 m/s	3 m/s	JEDEC PCB
YEB	$R_{\theta JA}$	161.14	144.57	137.07	131.95	2S2P
0.85 x 0.85	$R_{\theta JA}$	304.51	229.93	202.24	186.62	1S0P
4-Bump	$R_{\theta JB}$	76.54				2S2P
	$R_{\theta JC}$	77.05				1S0P
YEU	$R_{\theta JA}$	129.93	114.51	108.26	104.06	2S2P
0.95 x 1.25	$R_{\theta JA}$	247.84	183.41	160.92	148.31	1S0P
5-Bump	$R_{\theta JB}$	51.10				2S2P
	$R_{\theta JC}$	54.29				1S0P
YEC	$R_{\theta JA}$	126.383	110.04	103.98	99.88	2S2P
0.85 x 1.35	$R_{\theta JA}$	257.80	185.03	160.88	147.45	1S0P
6-Bump	$R_{\theta JB}$	53.26				2S2P
	$R_{\theta JC}$	55.97				1S0P
YED	$R_{\theta JA}$	107.58	92.58	87.42	84.02	2S2P
0.85 x 1.85	$R_{\theta JA}$	231.09	163.62	142.04	130.14	1S0P
8-Bump	$R_{\theta JB}$	43.16				2S2P
	$R_{\theta JC}$	39.27				1S0P
YEF	$R_{\theta JA}$	105.44	91.54	86.29	82.79	2S2P
1.35 x 1.35	$R_{\theta JA}$	215.45	148.93	127.01	114.92	1S0P
9-Bump	$R_{\theta JB}$	35.11				2S2P
	$R_{\theta JC}$	38.49				1S0P
YEG	$R_{\theta JA}$	88.99	75.31	70.55	67.43	2S2P
1.85 x 1.35	$R_{\theta JA}$	202.89	136.15	115.95	104.98	1S0P
12-Bump	$R_{\theta JB}$	31.83				2S2P
	$R_{\theta JC}$	26.20				1S0P
YEH	$R_{\theta JA}$	75.96	66.86	62.23	59.29	2S2P
1.85 x 1.85	$R_{\theta JA}$	185.51	121.93	103.31	93.19	1S0P
16-Bump	$R_{\theta JB}$	26.59				2S2P
	$R_{\theta JC}$	22.75				1S0P
YEJ	$R_{\theta JA}$	70.89	61.79	59.05	57.36	2S2P
1.85 x 2.35	$R_{\theta JA}$	173.48	112.28	94.55	85.08	1S0P
20-Bump	$R_{\theta JB}$	20.47				2S2P
	$R_{\theta JC}$	17.55				1S0P

NOTE 1: Per JESD 51−7 [4], and JESD 51−3 [5], Power = 1W

Table 2. Simulated Thermal Resistance Data(1) (continued)

	(°C/W)	0 m/s	1 m/s	2 m/s	3 m/s	JEDEC PCB
YEK	$R_{\theta JA}$	57.87	51.59	48.14	45.85	2S2P
2.35 x 2.35	$R_{\theta JA}$	162.01	105.30	90.28	80.22	1S0P
25-Bump	$R_{\theta JB}$	18.86				2S2P
	$R_{\theta JC}$	14.14				1S0P
YEL	$R_{\theta JA}$	55.02	48.33	45.42	43.50	2S2P
2.35 x 2.85	$R_{\theta JA}$	147.42	97.49	82.42	74.33	1S0P
30-Bump	$R_{\theta JB}$	17.98				2S2P
	$R_{\theta JC}$	12.32				1S0P
YEM	$R_{\theta JA}$	47.49	45.50	43.49	42.19	2S2P
2.85 x 2.85	$R_{\theta JA}$	141.41	90.60	74.02	65.47	1S0P
36-Bump	$R_{\theta JB}$	15.26				2S2P
	$R_{\theta JC}$	10.34				1S0P

NOTE 1: Per JESD 51−7 [4], and JESD 51−3 [5], Power = 1W

2.4 Board Level Reliability

The Texas Instruments packaging development team has performed extensive board-level reliability (BLR) testing on the NanoStar WCSP. These board-level reliability tests are in addition to standard device performance testing. A summary of the package-level tests and the passing criteria for WCSP are given in Table 3.

Table 3. Board-Level Reliability Test Matrix

Test	Condition	Criteria	Sample Size
Temperature Cycle	−40 to +125°C, 1 cycle/hr, 15 min. ramp(1)	1000 cycles, R < 1.2x from R_0	36
Temperature Shock	−40 to +125°C, 2 cycle/hr, 5 min. ramp(2)	500 cycle minimum, R < 1.2x from R_0	36
Drop	0.5m, 2000+με(3) measured impact	10 drops, R < 1.2x from R_0	5
Key Push	100 cycle/min., 20N max force, 1300με(3), Displacement = 2.7mm max	20K cycles, R < 1.2x from R_0	5
Three-Point Bend	Strain Rate 5mm/min. 100mm span	R < 1.2x from R_0 (35mm maximum)	5

NOTE 1: Per JEDEC JESD22−A104B Condition G [6]
NOTE 2: Per IPC-9701
NOTE 3: με = microstrain

In order to simplify the BLR testing, TI developed several different daisy-chain test devices. Separate devices were created to test both BOP and RDL technologies. The principal test vehicle configuration used was a N25, 5x5 array pattern. Information on the configuration of these devices is shown in Figure 8 and Figure 9.

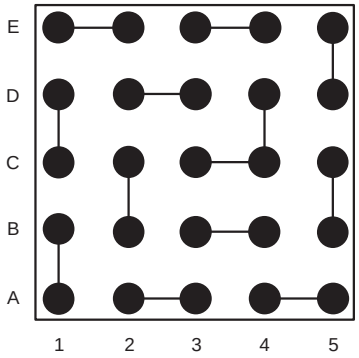


Figure 8. N25 5x5 Pin Array, 3.1mm Square, Daisy-Chain Test Die Diagram

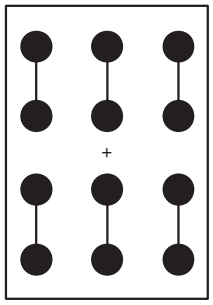


Figure 9. N12 3x4 Pin Array, 2.14mm x 1.5mm, Daisy-Chain Test Die Diagram

The DC devices were mounted on 160°C glass transition laminate PCBs for testing. Figure 10 shows an example of one of these test boards. These test PCBs were used for all thermal cycle BLR testing. All devices were tested using a thermal cycle with less than a 5-minute ramp, and were continuously monitored during testing. Those test boards placed into the 15-minute ramp temperature cycle were checked at ~65 cycle intervals. Summary thermal cycle testing failure data is provided in Table 4.

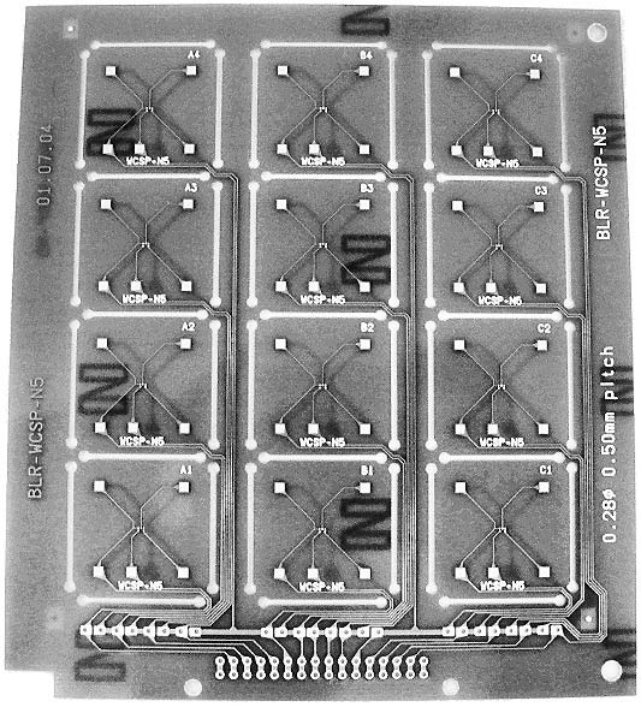


Figure 10. 12-Site Thermal Cycle Test BLR Test Board

Table 4. NanoStar Board Level Reliability Summary

Test	Vehicle					
	N25 Tin-Lead		N25 Lead-Free		N12 Tin-Lead	
	1st Fail	63% Weibull Life	1st Fail	63% Weibull Life	1st Fail	63% Weibull Life
Temperature Cycle	1660 Cycles	2502 Cycles	1389 Cycles	2301 Cycles	1827 Cycles	+2579(1)
Temperature Shock	1177 Cycles	1850 Cycles	1515 Cycles	2326 Cycles	1516 Cycles	3885 Cycles
Drop	123 Drops	208 Drops	101 Drops	160 Drops	223 Drops	548 Drops
Key Push	0/8 Fail	451301 Cycles	0/8 Fail	1.24M Cycles	0/8 Fail	651160 Cycles
Three-Point Bend	N/A	Maximum	N/A	Maximum	N/A	Maximum

NOTE 1: Test stopped at 2579 cycles due to chamber malfunction.

The NanoStar WCSP BLR testing demonstrated excellent reliability in all testing. The BLR Weibull graph shows the difference achieved by using different thermal cycle profiles. As shown in Figure 11, the Weibull slope increased and the N63 fatigue life decreased as the thermal ramp temperature rate increased. Additionally, the graph shows significant improvement in a fatigue cycle file between brittle polymeric materials and TI's new re-passivation polymer technology. Also, the cycle life increases as the array size on WCSP decreases. This finding is shown by the increased performance exhibited by the N12 device.

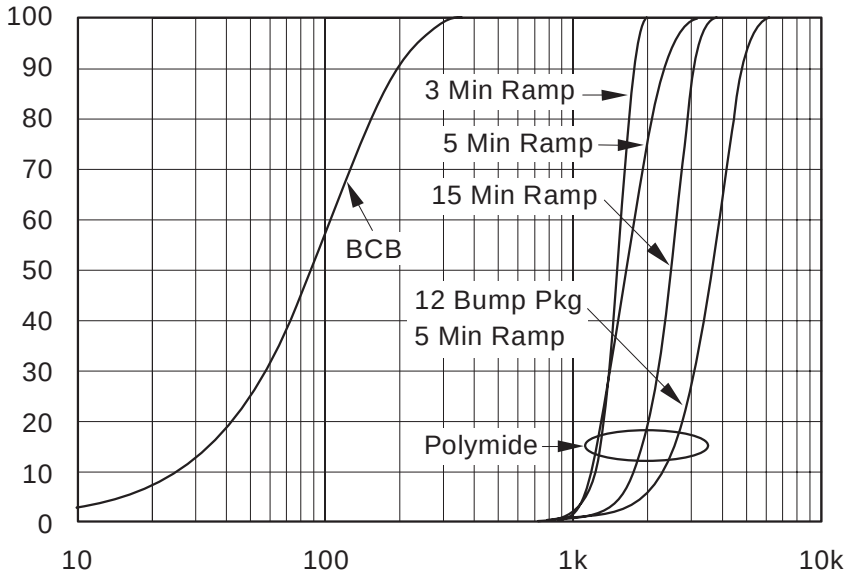


Figure 11. N25 TCT Weibull Comparison of Ramp Rates and Materials

Cross-sectional images of NanoStar BLR failures are shown in Figure 12 through Figure 15. The images display typical solder cracks for BLR failures obtained with both tin-lead and lead-free solder.

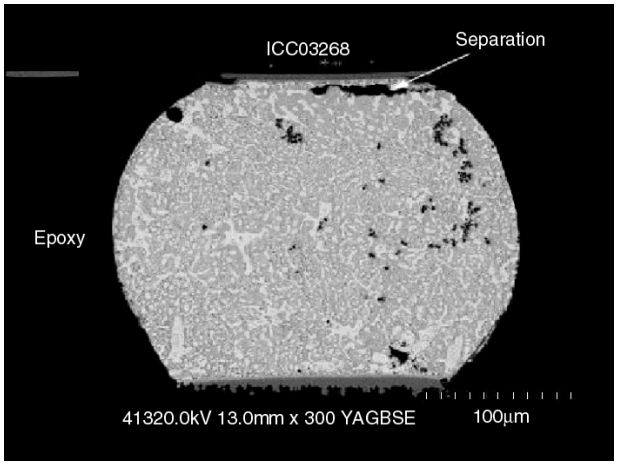


Figure 12. Typical Tin-Lead BLR Solder Fatigue Crack

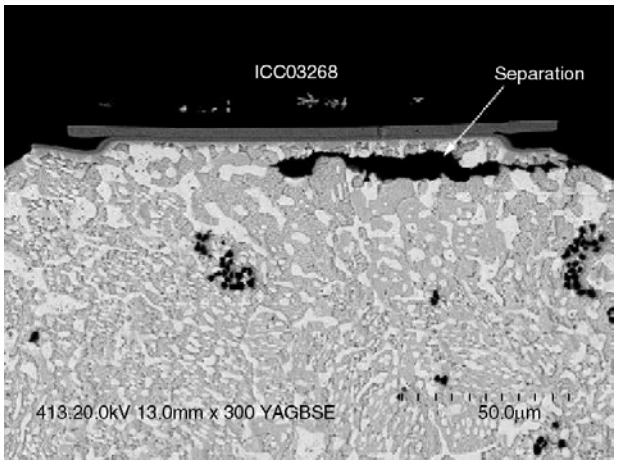


Figure 13. Enlargement of Crack Area in Figure 12

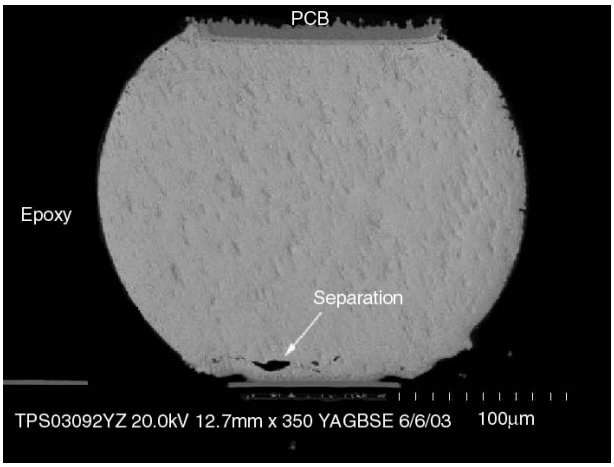


Figure 14. Typical Lead-Free BLR Solder Fatigue Crack

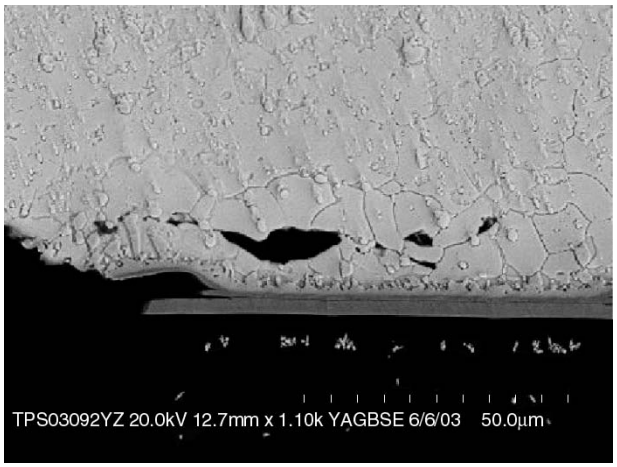


Figure 15. Enlargement of Crack Area in Figure 14

3 Printed Circuit Board Assembly

NanoStar can be assembled with normal SMT assembly practices in solder paste print, component placement, and reflow. This section provides detailed recommendations to achieve best overall performance.

3.1 PCB Design Guidelines

The size of WCSP requires care in the PCB design process for optimum reliability, processing, and manufacturability. In addition to the land pattern information (see section 3.2), the following rules should be observed:

- Best reliability results are achieved when the PCB laminate glass transition temperature is above the operating range of the intended application.

- For PCBs using a Ni/Au surface finish, the gold thickness should be less 0.5µm to avoid a reduction in solder joint thermal fatigue performance.
- Ni/Au surface finishes are not recommended for use with lead-free solder devices. OSP surface finish will deliver superior reliability results.
- Trace routing away from WCSP device should be balanced in ***x*** and ***y*** directions to avoid unintentional component movement as a result of unbalanced solder wetting forces. (An example of this effect can be seen in Figure 16.)
- Solder-mask thickness should be less than 1 mil (.001in) on top of the copper circuit pattern.
- Circuit traces routed away from PCB land pads should be less than 100µm wide (preferably ≈ 75µm) in the exposed area inside the solder mask opening. Wider trace widths will reduce device stand-off and impact reliability.
- Recommended solder paste is Type 3.

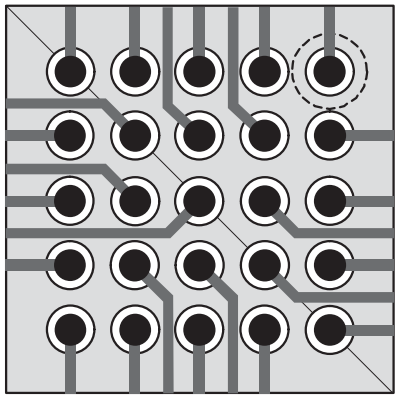


Figure 16. Example of 5x5 Array Balanced Routing Pattern

3.2 PCB Land Pattern Recommendations

The recommended land pattern for all NanoStar solder pads is a Non-Solder-Mask defined (NMSD) solder pad. The size and shape recommendation for all devices is identical, and is given in Figure 17. Recommended dimensions are provided in Table 5.

Table 5. Recommended PCB Solder Land Pattern

Solder Pad Definition	Copper Pad	Solder Mask Opening	Copper Thickness
Non-Solder-Mask Defined (NMSD)	275µm (+0.0, −25µm)	375µm (+0.0, −25µm)	1oz max (32µm)

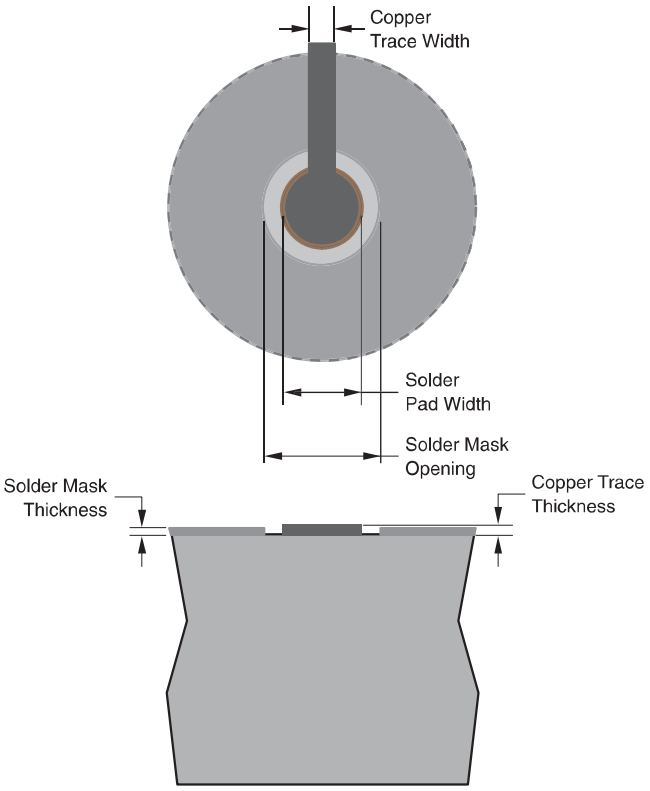


Figure 17. Recommended Solder Land Pattern Outline

3.3 Solder Paste Stencil Design

Stencil design for NanoStar should follow standard industry recommendations such as IPC-7525 *Stencil Design Guidelines* [7]. Best BLR performance is achieved when maximum device standoff exists, which is obtained with maximum manufacturable solder paste volume. The solder stencil opening is identical for all solder pads in a WCSP array. Recommended stencil information is found in Table 6.

Table 6. Recommended Solder Stencil Pattern

Stencil Opening(1)	Stencil Thickness(2)
300µm Round, or 275µm x 275µm Square	100−125µm thick

NOTE 1: Round stencil opening preferred.
NOTE 2: Best solder stencil performance will be achieved using laser cut stencils with electro-polishing. The use of chemically etched stencils results in inferior solder paste volume control.

3.4 Component Placement

Typical surface mount placement equipment capable of placing similar sized SMT devices can assemble the NanoStar WCSP. The package provides robust self-alignment, and will re-center with up to 150µm of displacement. There is one recommendation concerning placement force for best successwith component placement processes, however.

- On equipment without component force adjustments, the ***Z*** placement height should be set to avoid overdriving the board location. Optimally, the ***Z*** height should be set at one-half the printed solder paste height.

- On equipment with component placement force adjustments, the maximum recommended placement force is 35g/bump. Exceeding this force level can reduce reliability due to excessive silicon impact stress and subsequent damage.

3.5 Reflow

Recommended solder reflow profiles for NanoStar are shown in Figure 18. Critical reflow temperatures are given in Table 7.

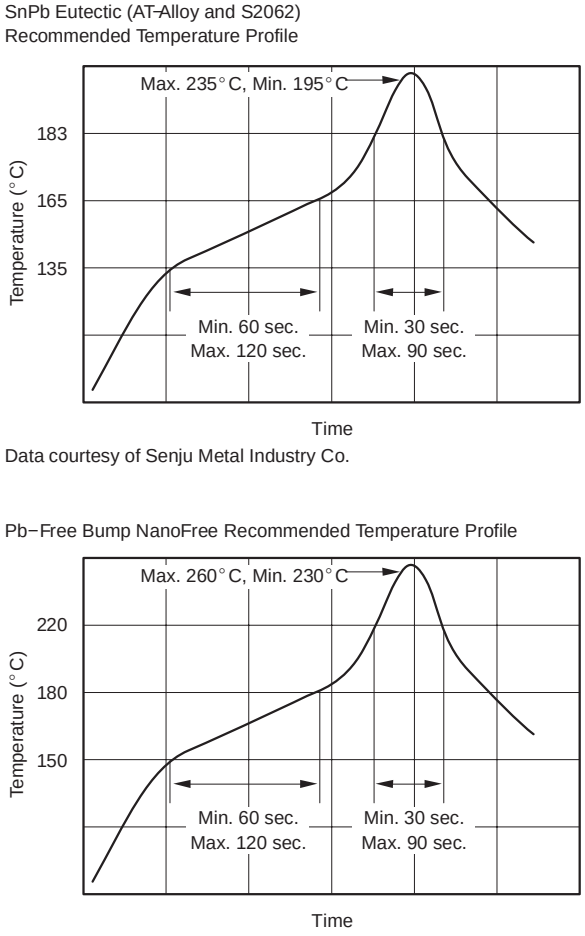


Figure 18. Recommended Reflow Profiles

Table 7. Recommended Critical Reflow Parameters

Process Step	Tin-Lead Solder	Lead-Free Solder
Ramp Rate	3°C/sec Maximum	3°C/sec
Pre-Heat	165°C, 60 to 120 seconds	Max. 150°C to 180°C, 60 to 180 seconds
Time above Liquidus	183°C, 30 to 90 seconds	220°C, 30 to 90 seconds
Peak Temperature	235°C	255°C ±5°C
Time within 5°C of Peak Temperature	10 to 20 seconds	10 to 20 seconds
Ramp Down Rate	6°C/sec Maximum	6°C/sec Maximum

4 Tape and Reel Information

4.1 Material Specifications

TI offers tape-and-reel packing for NanoStar packages in standard packing quantities (SPQ) of 250 and 3000 units/reel. The units are shipped in embossed carrier tape, sealed with heat-activated or pressure-sensitive cover tape, and wound on plastic reels. All of the tape-and-reel materials comply with EIA−481, and EIA−541 [8, 9]. The EIA specifications are shown in Figure 19 and Figure 20, as well as in Table 8 and Table 9. The carrier tape is made of conductive polystyrene and has a surface resistivity that falls within the static-dissipative range (1×10^5 to $1\times10^{11}\Omega^2$). Heat-activated or pressure-sensitive, antistatic, clear polyester film is used for the cover tape. The dimensions of most interest to the end user are tape width (W), cavity pitch (P), and cavity size (A_0, B_0, K_0), as shown in Figure 19. Due to the wide range of die sizes within a given array size, the cavity size dimensions will vary. Please refer to the specific product data sheet for devices of interest for the cavity dimensions (A_0, B_0, K_0).

The units are placed in the carrier-tape cavity, with pin 1 located as specified in EIA−481. The longest axis of the package is perpendicular to the tape sprocket holes, and pin 1 is closest to the round sprocket holes. Thus, for rectangular or square packages, pin 1 is located in quadrant 1 (see Figure 21). All dimensions are in millimeters.

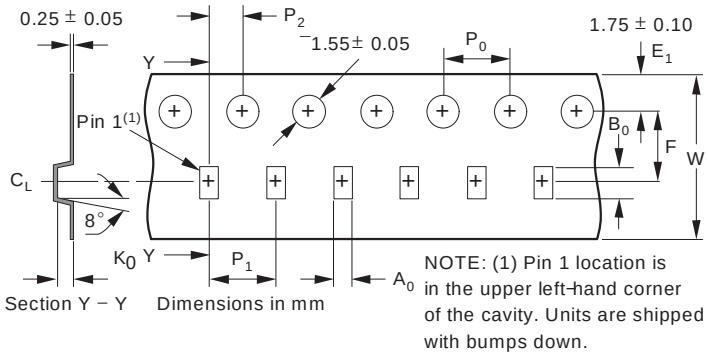
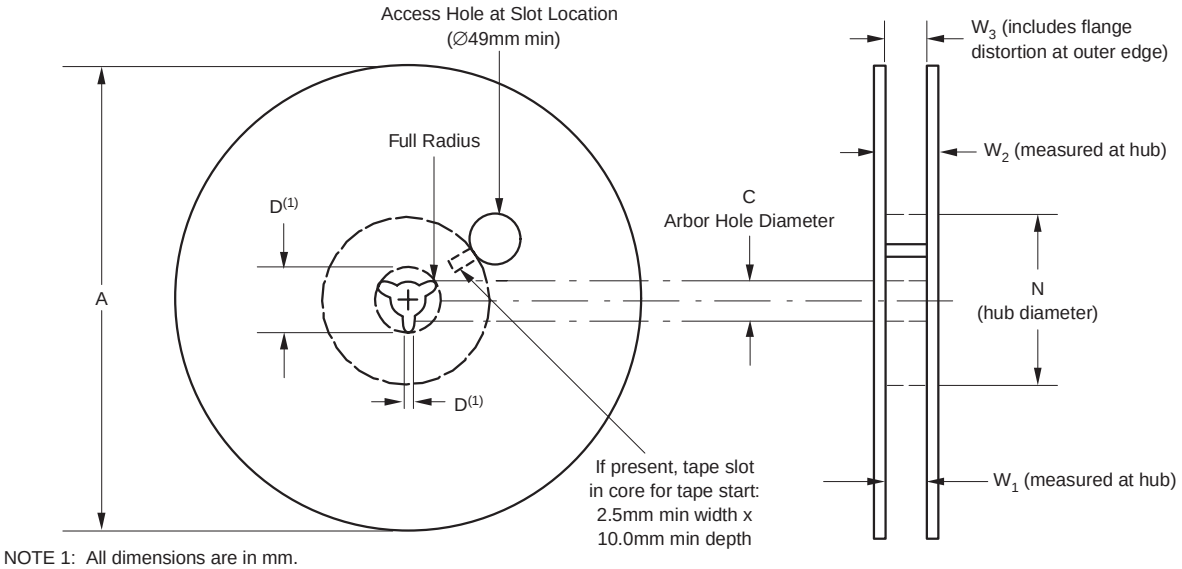


Figure 19. Pocket Tape Dimensions

Table 8. Common Tape Dimensions by Designator(1)

Designator	YEB	YEC	YED	YEF	YEG	YEH	YEJ	YEK	YEL	YEM
Pocket Pitch, P_1	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10	8.00 ± .10	8.00 ± .10	8.00 ± .10	8.00 ± .10
Sprocket Hole-to-Pocket Centerline, F	3.50 ± .05	3.50 ± .05	3.50 ± .05	3.50 ± .05	3.50 ± .05	3.50 ± .05	5.50 ± .05	5.50 ± .05	5.50 ± .05	5.50 ± .05
Sprocket Hole-to-Pocket Offset, P_2	2.00 ± .05	2.00 ± .05	2.00 ± .05	2.00 ± .05	2.00 ± .05	2.00 ± .05	2.00 ± .05	2.00 ± .05	2.00 ± .05	2.00 ± .05
Sprocket Hole Pitch, P_0	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10	4.00 ± .10
Tape Width, W	8	8	8	8	8	8	12	12	12	12
Reel Diameter, Max.	178	178	178	178	178	178	178 / 330	178 / 330	178 / 330	178 / 330

NOTE 1: All dimensions are in mm.



NOTE 1: All dimensions are in mm.

Figure 20. Pocket Tape Dimensions

Table 9. Reel Specifications(1)

Reel Diameter (A)	Reel Width (W1)	Hub Diameter Max (N)	Reel Thickness (W2)	Arbor-Hole Diameter (C)	Quantity/Reel
178 ± 0.60	8.4 ± 1.65	62 ± 0.50	14.4 ± 1.65	13.0 ± 0.5/–0.2	250 or 3000
178 ± 0.60	12.4 ± 1.65	62 ± 0.50	18.4 ± 1.65	13.0 ± 0.5/–0.2	250
330 ± 0.60	12.4 ± 1.65	62 ± 0.50	18.4 ± 1.65	13.0 ± 0.5/–0.2	3000

NOTE 1: All dimensions are in mm.

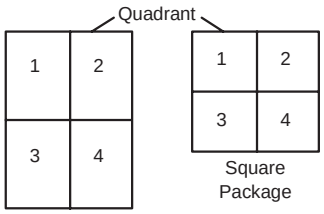


Figure 21. Carrier-Tape Cavity Quadrant Location for Pin 1, per EIA−481B

5 Symbolization

The top of the package is laser-marked with device name, date code, assembly-site code, assembly-lot trace code, and pin-1 location as space allows. Table 10 shows the device-marking symbolization guidelines for NanoStar packages.

The ***Character*** and ***WCSP Laser Mark Image*** column entries in Table 10 have the following meanings:

CCCC Device name (shortened in accordance with product data sheet)

Y Year

M Month

D Day

S Site code

LLLL Lot trace code

A Pin-1 quadrant identifier (data sheet specifies exact pin-1 location)

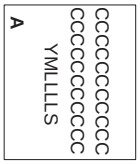
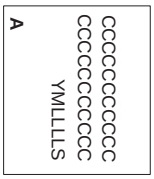
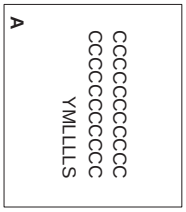
Tin-lead solder devices use a “1” (one), and lead-free solder devices use a “0” (zero).

For specific marking information on a particular device, please see the device data sheet (available for download from the TI web site).

Table 10. Device-Marking Guidelines

Designator	Text Rows	Characters	WCSP Laser Mark Image
YEB YZB 4YZT	1	Lot Code and 2-Character Device Code	A YMDS CC
YEA/YZA YEP/YZT 5YZT/6YZT YEC/YZC YEQ/YZQ YEU/YZU	1	Lot Code and 2-Character Device Code	A YMDCCS
YED YZD	0	Full Lot Code No Device Code	A YMLLLLS

Table 10. Device-Marking Guidelines (continued)

Designator	Text Rows	Characters	WCSP Laser Mark Image
YEF YZF	2	Full Lot Code and 3-Character Device Code	
YEG YZG	2	Full Lot Code and 6-Character Device Code	
YEH YZH	3	Full Lot Code and 8-Character Device Code	
YEJ YZJ	3	Full Lot Code and up to 22-Character Device Code	
YEK YZK	3	Full Lot Code and up to 22-Character Device Code	
YEL YZL	3	Full Lot Code and up to 22-Character Device Code	
YEM YZM	3	Full Lot Code and up to 22-Character Device Code	

6 Features and Benefits

In summary, key features and advantages for devices in the NanoStar package are:

- Smallest possible form factor; die size equals package size.
- Excellent proven board level reliability performance
- Compatible with standard SMT assembly processes.
- Compatible with standard surface mount PCB technology.

7 Conclusion

Texas Instruments NanoStar package offerings are bare die packages, with improved performance and reduced package footprint over similar SOT-23, SC-70, and SOIC packages. Additionally, the NanoStar packages meet the industry's lead-free demands, have reliable solderability using either lead or lead-free solder paste, and can be reworked and manufactured using conventional equipment. The packages allow for product miniaturization and comply with dimensional specifications of JEDEC standard MO−211.

Acknowledgments

The author wishes to thank the entire NanoStar development team. This package would not have been possible without the support of each and every person on the worldwide WCSP team. Unfortunately, the list of contributors is too large for print.

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Listed JEDEC references can be found at: http://www.jedec.org/download/default.cfm.

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