AND9275, Rev. 3

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AR0141CS Register Reference

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Introduction

This reference document describes the AR0141CS registers. Summary and detailed information are presented in separate sections:

- “Manufacturer-Specific Register List and Default Values” on page 5
- “Manufacturer Specific Register Descriptions” on page 16

Note: Throughout this document, Green1 to corresponds to greenR; green2 corresponds to greenB.

How to Access Registers

All the registers can be accessed by the two-wire serial interface with 16-bit addresses and 16-bit data.

For more detailed information on the interface protocol of the two-wire serial interface, see the AR0141CS data sheet.

Reserved Registers

All the reserved bits should not be changed. The user must write the original values back when changing the registers.

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck (R0x300C-D) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

By default, bad frames are not masked. In the register tables, the “Bad Frame” column shows where changing a register or register field will cause a bad frame. This notation is used:

N—No. Changing the register value will not produce a bad frame.

Y—Yes. Changing the register value might produce a bad frame.

YM—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x3023) is set to “1.”

Register Map

The tables in this section show which locations are used within the 16-bit address space. Locations that are not shown in the table are reserved for future use; to maintain compatibility with future designs they should not be read from or written to. Locations that are shown as “Reserved” should not be accessed. The default read values of registers are subject to change.

Caution **The effect of writing to reserved registers is undefined and includes the possibility of causing permanent electrical damage to the sensor.**

Table 1 below lists registers and their default values. Register addresses are shown as 16-bit values in both decimal and hexadecimal. Table 2 on page 16 lists registers and their descriptions.

Manufacturer-Specific Register List and Default Values

Table 1: Manufacturer-Specific Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12288 (R0x3000)	chip_version_reg	dddd dddd dddd dddd	337 (0x0151)
R12290 (R0x3002)	y_addr_start	0000 00dd dddd dddd	64 (0x0040)
R12292 (R0x3004)	x_addr_start	0000 0ddd dddd dddd	18 (0x0012)
R12294 (R0x3006)	y_addr_end	0000 00dd dddd dddd	791 (0x0317)
R12296 (R0x3008)	x_addr_end	0000 0ddd dddd dddd	1305 (0x0519)
R12298 (R0x300A)	frame_length_lines	dddd dddd dddd dddd	750 (0x02EE)
R12300 (R0x300C)	line_length_pck	dddd dddd dddd dddd	1650 (0x0672)
R12302 (R0x300E)	revision_number	dddd dddd	0 (0x00)
R12304 (R0x3010)	lock_control	dddd dddd dddd dddd	48879 (0xBEEF)
R12306 (R0x3012)	coarse_integration_time	dddd dddd dddd dddd	16 (0x0010)
R12308 (R0x3014)	fine_integration_time	dddd dddd dddd dddd	0 (0x0000)
R12310 (R0x3016)	coarse_integration_time_cb	dddd dddd dddd dddd	16 (0x0010)
R12312 (R0x3018)	fine_integration_time_cb	dddd dddd dddd dddd	0 (0x0000)
R12314 (R0x301A)	reset_register	d00d dddd dddd dddd	88 (0x0058)
R12316 (R0x301C)	mode_select_	0000 000d	0 (0x00)

Table 1: Manufacturer-Specific Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12317 (R0x301D)	image_orientation_	0000 00dd	0 (0x00)
R12318 (R0x301E)	data_pedestal	0000 dddd dddd dddd	168 (0x00A8)
R12321 (R0x3021)	software_reset_	0000 000d	0 (0x00)
R12322 (R0x3022)	grouped_parameter_hold_	0000 000d	0 (0x00)
R12323 (R0x3023)	mask_corrupted_frames_	0000 000d	0 (0x00)
R12324 (R0x3024)	pixel_order_	0000 00??	0 (0x00)
R12326 (R0x3026)	gpi_status	dddd dddd dddd ????	25856 (0x6500)
R12328 (R0x3028)	row_speed	0000 0000 0ddd 0000	16 (0x0010)
R12330 (R0x302A)	vt_pix_clk_div	0000 0000 000d dddd	6 (0x0006)
R12332 (R0x302C)	vt_sys_clk_div	0000 0000 000d dddd	1 (0x0001)
R12334 (R0x302E)	pre_pll_clk_div	0000 0000 00dd dddd	4 (0x0004)
R12336 (R0x3030)	pll_multiplier	0000 0000 dddd dddd	66 (0x0042)
R12342 (R0x3036)	op_pix_clk_div	0000 0000 000d dddd	12 (0x000C)
R12344 (R0x3038)	op_sys_clk_div	0000 0000 000d dddd	2 (0x0002)
R12346 (R0x303A)	frame_count	???? ???? ???? ????	65535 (0xFFFF)
R12348 (R0x303C)	frame_status	0000 0000 0000 ????	0 (0x0000)
R12350 (R0x303E)	line_length_pck_cb	dddd dddd dddd dddd	1650 (0x0672)
R12352 (R0x3040)	read_mode	dddd dd00 0ddd 0000	0 (0x0000)
R12354 (R0x3042)	extra_delay	dddd dddd dddd dddd	0 (0x0000)
R12358 (R0x3046)	flash	??d0 000d d0dd dddd	0 (0x0000)
R12360 (R0x3048)	flash2	dddd dddd dddd dddd	256 (0x0100)
R12374 (R0x3056)	green1_gain	0000 0ddd dddd dddd	128 (0x0080)
R12376 (R0x3058)	blue_gain	0000 0ddd dddd dddd	128 (0x0080)
R12378 (R0x305A)	red_gain	0000 0ddd dddd dddd	128 (0x0080)

Table 1: Manufacturer-Specific Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12380 (R0x305C)	green2_gain	0000 0ddd dddd dddd	128 (0x0080)
R12382 (R0x305E)	global_gain	0000 0ddd dddd dddd	128 (0x0080)
R12384 (R0x3060)	analog_gain	dddd dddd 0ddd dddd	0 (0x0000)
R12388 (R0x3064)	smia_test	000d dddd d000 dddd	6530 (0x1982)
R12398 (R0x306E)	datapath_select	dddd dddd 000d 00dd	36880 (0x9010)
R12400 (R0x3070)	test_pattern_mode	0000 00dd 0000 0ddd	0 (0x0000)
R12402 (R0x3072)	test_data_red	0000 dddd dddd dddd	0 (0x0000)
R12404 (R0x3074)	test_data_greenr	0000 dddd dddd dddd	0 (0x0000)
R12406 (R0x3076)	test_data_blue	0000 dddd dddd dddd	0 (0x0000)
R12408 (R0x3078)	test_data_greenb	0000 dddd dddd dddd	0 (0x0000)
R12410 (R0x307A)	test_raw_mode	0000 0000 0000 00dd	0 (0x0000)
R12422 (R0x3086)	seq_data_port	dddd dddd dddd dddd	0 (0x0000)
R12424 (R0x3088)	seq_ctrl_port	?d00 00dd dddd dddd	49152 (0xC000)
R12426 (R0x308A)	x_addr_start_cb	0000 0ddd dddd dddd	18 (0x0012)
R12428 (R0x308C)	y_addr_start_cb	0000 00dd dddd dddd	64 (0x0040)
R12430 (R0x308E)	x_addr_end_cb	0000 0ddd dddd dddd	1305 (0x0519)
R12432 (R0x3090)	y_addr_end_cb	0000 00dd dddd dddd	791 (0x0317)
R12448 (R0x30A0)	x_even_inc	0000 0000 0000 000?	1 (0x0001)
R12450 (R0x30A2)	x_odd_inc	0000 0000 0000 0ddd	1 (0x0001)
R12452 (R0x30A4)	y_even_inc	0000 0000 0000 000?	1 (0x0001)
R12454 (R0x30A6)	y_odd_inc	0000 0000 0000 0ddd	1 (0x0001)
R12456 (R0x30A8)	y_odd_inc_cb	0000 0000 0000 0ddd	1 (0x0001)
R12458 (R0x30AA)	frame_length_lines_cb	dddd dddd dddd dddd	750 (0x02EE)
R12462 (R0x30AE)	x_odd_inc_cb	0000 0000 0000 0ddd	1 (0x0001)

Table 1: Manufacturer-Specific Register List

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12464 (R0x30B0)	digital_test	0dd0 0000 d00d dd0d	0 (0x0000)
R12466 (R0x30B2)	tempsens_data	0000 00dd dddd dddd	0 (0x0000)
R12468 (R0x30B4)	tempsens_ctrl	dddd dddd dddd dddd	0 (0x0000)
R12470 (R0x30B6)	spare_0x30b6	dddd dddd dddd dddd	0 (0x0000)
R12472 (R0x30B8)	spare_0x30b8	dddd dddd dddd dddd	0 (0x0000)
R12474 (R0x30BA)	digital_ctrl	0000 000d 00d0 dddd	44 (0x002C)
R12476 (R0x30BC)	green1_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12478 (R0x30BE)	blue_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12480 (R0x30C0)	red_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12482 (R0x30C2)	green2_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12484 (R0x30C4)	global_gain_cb	0000 0ddd dddd dddd	128 (0x0080)
R12486 (R0x30C6)	tempsens_calib1	dddd dddd dddd dddd	291 (0x0123)
R12488 (R0x30C8)	tempsens_calib2	dddd dddd dddd dddd	17767 (0x4567)
R12490 (R0x30CA)	tempsens_calib3	dddd dddd dddd dddd	35243 (0x89AB)
R12492 (R0x30CC)	tempsens_calib4	dddd dddd dddd dddd	52719 (0xCDEF)
R12494 (R0x30CE)	grr_control1	0000 000d dddd 0d0d	0 (0x0000)
R12496 (R0x30D0)	grr_control2	0000 0000 dddd dddd	5 (0x0005)
R12498 (R0x30D2)	grr_control3	dddd dddd dddd dddd	4 (0x0004)
R12506 (R0x30DA)	grr_control4	dddd dddd dddd dddd	10 (0x000A)
R12544 (R0x3100)	aectrlreg	0000 0000 d000 0d00	0 (0x0000)
R12608 (R0x3140)	ae_roi_x_start_offset	0000 0ddd dddd ddd0	0 (0x0000)
R12610 (R0x3142)	ae_roi_y_start_offset	0000 00dd dddd ddd0	0 (0x0000)
R12612 (R0x3144)	ae_roi_x_size	0000 0ddd dddd ddd0	1288 (0x0508)
R12614 (R0x3146)	ae_roi_y_size	0000 00dd dddd ddd0	728 (0x02D8)

Table 1: Manufacturer-Specific Register List

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12616 (R0x3148)	ae_hist_begin_perc	dddd dddd dddd dddd	656 (0x0290)
R12618 (R0x314A)	ae_hist_end_perc	dddd dddd dddd dddd	65528 (0xFFF8)
R12620 (R0x314C)	ae_hist_div	dddd dddd dddd dddd	256 (0x0100)
R12622 (R0x314E)	ae_norm_width_min	dddd dddd dddd dddd	32 (0x0020)
R12624 (R0x3150)	ae_mean_h	0000 0000 0000 ????	0 (0x0000)
R12626 (R0x3152)	ae_mean_l	???? ???? ???? ????	0 (0x0000)
R12628 (R0x3154)	ae_hist_begin_h	0000 0000 0000 ????	0 (0x0000)
R12630 (R0x3156)	ae_hist_begin_l	???? ???? ???? ????	0 (0x0000)
R12632 (R0x3158)	ae_hist_end_h	0000 0000 0000 ????	0 (0x0000)
R12634 (R0x315A)	ae_hist_end_l	???? ???? ???? ????	0 (0x0000)
R12636 (R0x315C)	ae_low_end_mean_h	0000 0000 0000 ????	0 (0x0000)
R12638 (R0x315E)	ae_low_end_mean_l	???? ???? ???? ????	0 (0x0000)
R12640 (R0x3160)	ae_perc_low_end	???? ???? ???? ????	0 (0x0000)
R12642 (R0x3162)	ae_norm_abs_dev	???? ???? ???? ????	0 (0x0000)
R12716 (R0x31AC)	data_format_bits	000d dddd 000d dddd	3084 (0x0C0C)
R12718 (R0x31AE)	serial_format	0000 00dd 0000 0ddd	772 (0x0304)
R12736 (R0x31C0)	hispi_timing	dddd dddd dddd dddd	32768 (0x8000)
R12738 (R0x31C2)	hispi_blanking	dddd dddd dddd dddd	65535 (0xFFFF)
R12740 (R0x31C4)	hispi_sync_patt	dddd dddd dddd dddd	62805 (0xF555)
R12742 (R0x31C6)	hispi_control_status	??dd dddd dddd dddd	32768 (0x8000)
R12744 (R0x31C8)	hispi_crc_0	???? ???? ???? ????	0 (0x0000)
R12746 (R0x31CA)	hispi_crc_1	???? ???? ???? ????	0 (0x0000)
R12748 (R0x31CC)	hispi_crc_2	???? ???? ???? ????	0 (0x0000)
R12750 (R0x31CE)	hispi_crc_3	???? ???? ???? ????	0 (0x0000)

Table 1: Manufacturer-Specific Register List

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R12752 (R0x31D0)	companding	0000 0000 0000 000d	1 (0x0001)
R12754 (R0x31D2)	stat_frame_id	dddd dddd dddd dddd	0 (0x0000)
R12758 (R0x31D6)	i2c_wrt_checksum	dddd dddd dddd dddd	65535 (0xFFFF)
R12776 (R0x31E8)	horizontal_cursor_position	0000 00dd dddd dddd	0 (0x0000)
R12778 (R0x31EA)	vertical_cursor_position	0000 0ddd dddd dddd	0 (0x0000)
R12780 (R0x31EC)	horizontal_cursor_width	0000 00dd dddd dddd	0 (0x0000)
R12782 (R0x31EE)	vertical_cursor_width	0000 0ddd dddd dddd	0 (0x0000)
R12788 (R0x31F4)	fuse_id1	dddd dddd dddd dddd	0 (0x0000)
R12790 (R0x31F6)	fuse_id2	dddd dddd dddd dddd	0 (0x0000)
R12792 (R0x31F8)	fuse_id3	dddd dddd dddd dddd	0 (0x0000)
R12794 (R0x31FA)	fuse_id4	dddd dddd dddd dddd	0 (0x0000)
R12796 (R0x31FC)	cci_ids	dddd dddd dddd dddd	12320 (0x3020)
R12800 (R0x3200)	adacd_control	0000 0000 0000 00dd	0 (0x0000)
R12802 (R0x3202)	adacd_noise_model1	0000 00dd dddd dddd	140 (0x008C)
R12806 (R0x3206)	adacd_noise_floor1	dddd dddd dddd dddd	1027 (0x0403)
R12808 (R0x3208)	adacd_noise_floor2	dddd dddd dddd dddd	2566 (0x0A06)
R12810 (R0x320A)	adacd_pedestal	0000 dddd dddd dddd	128 (0x0080)
R13824 (R0x3600)	p_gr_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13826 (R0x3602)	p_gr_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13828 (R0x3604)	p_gr_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13830 (R0x3606)	p_gr_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13832 (R0x3608)	p_gr_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13834 (R0x360A)	p_rd_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13836 (R0x360C)	p_rd_p0q1	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13838 (R0x360E)	p_rd_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13840 (R0x3610)	p_rd_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13842 (R0x3612)	p_rd_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13844 (R0x3614)	p_bl_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13846 (R0x3616)	p_bl_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13848 (R0x3618)	p_bl_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13850 (R0x361A)	p_bl_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13852 (R0x361C)	p_bl_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13854 (R0x361E)	p_gb_p0q0	dddd dddd dddd dddd	0 (0x0000)
R13856 (R0x3620)	p_gb_p0q1	dddd dddd dddd dddd	0 (0x0000)
R13858 (R0x3622)	p_gb_p0q2	dddd dddd dddd dddd	0 (0x0000)
R13860 (R0x3624)	p_gb_p0q3	dddd dddd dddd dddd	0 (0x0000)
R13862 (R0x3626)	p_gb_p0q4	dddd dddd dddd dddd	0 (0x0000)
R13888 (R0x3640)	p_gr_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13890 (R0x3642)	p_gr_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13892 (R0x3644)	p_gr_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13894 (R0x3646)	p_gr_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13896 (R0x3648)	p_gr_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13898 (R0x364A)	p_rd_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13900 (R0x364C)	p_rd_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13902 (R0x364E)	p_rd_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13904 (R0x3650)	p_rd_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13906 (R0x3652)	p_rd_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13908 (R0x3654)	p_bl_p1q0	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13910 (R0x3656)	p_bl_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13912 (R0x3658)	p_bl_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13914 (R0x365A)	p_bl_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13916 (R0x365C)	p_bl_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13918 (R0x365E)	p_gb_p1q0	dddd dddd dddd dddd	0 (0x0000)
R13920 (R0x3660)	p_gb_p1q1	dddd dddd dddd dddd	0 (0x0000)
R13922 (R0x3662)	p_gb_p1q2	dddd dddd dddd dddd	0 (0x0000)
R13924 (R0x3664)	p_gb_p1q3	dddd dddd dddd dddd	0 (0x0000)
R13926 (R0x3666)	p_gb_p1q4	dddd dddd dddd dddd	0 (0x0000)
R13952 (R0x3680)	p_gr_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13954 (R0x3682)	p_gr_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13956 (R0x3684)	p_gr_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13958 (R0x3686)	p_gr_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13960 (R0x3688)	p_gr_p2q4	dddd dddd dddd dddd	0 (0x0000)
R13962 (R0x368A)	p_rd_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13964 (R0x368C)	p_rd_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13966 (R0x368E)	p_rd_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13968 (R0x3690)	p_rd_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13970 (R0x3692)	p_rd_p2q4	dddd dddd dddd dddd	0 (0x0000)
R13972 (R0x3694)	p_bl_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13974 (R0x3696)	p_bl_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13976 (R0x3698)	p_bl_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13978 (R0x369A)	p_bl_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13980 (R0x369C)	p_bl_p2q4	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R13982 (R0x369E)	p_gb_p2q0	dddd dddd dddd dddd	0 (0x0000)
R13984 (R0x36A0)	p_gb_p2q1	dddd dddd dddd dddd	0 (0x0000)
R13986 (R0x36A2)	p_gb_p2q2	dddd dddd dddd dddd	0 (0x0000)
R13988 (R0x36A4)	p_gb_p2q3	dddd dddd dddd dddd	0 (0x0000)
R13990 (R0x36A6)	p_gb_p2q4	dddd dddd dddd dddd	0 (0x0000)
R14016 (R0x36C0)	p_gr_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14018 (R0x36C2)	p_gr_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14020 (R0x36C4)	p_gr_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14022 (R0x36C6)	p_gr_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14024 (R0x36C8)	p_gr_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14026 (R0x36CA)	p_rd_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14028 (R0x36CC)	p_rd_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14030 (R0x36CE)	p_rd_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14032 (R0x36D0)	p_rd_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14034 (R0x36D2)	p_rd_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14036 (R0x36D4)	p_bl_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14038 (R0x36D6)	p_bl_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14040 (R0x36D8)	p_bl_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14042 (R0x36DA)	p_bl_p3q3	dddd dddd dddd dddd	0 (0x0000)
R14044 (R0x36DC)	p_bl_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14046 (R0x36DE)	p_gb_p3q0	dddd dddd dddd dddd	0 (0x0000)
R14048 (R0x36E0)	p_gb_p3q1	dddd dddd dddd dddd	0 (0x0000)
R14050 (R0x36E2)	p_gb_p3q2	dddd dddd dddd dddd	0 (0x0000)
R14052 (R0x36E4)	p_gb_p3q3	dddd dddd dddd dddd	0 (0x0000)

Table 1: Manufacturer-Specific Register List
1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14054 (R0x36E6)	p_gb_p3q4	dddd dddd dddd dddd	0 (0x0000)
R14080 (R0x3700)	p_gr_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14082 (R0x3702)	p_gr_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14084 (R0x3704)	p_gr_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14086 (R0x3706)	p_gr_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14088 (R0x3708)	p_gr_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14090 (R0x370A)	p_rd_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14092 (R0x370C)	p_rd_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14094 (R0x370E)	p_rd_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14096 (R0x3710)	p_rd_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14098 (R0x3712)	p_rd_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14100 (R0x3714)	p_bl_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14102 (R0x3716)	p_bl_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14104 (R0x3718)	p_bl_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14106 (R0x371A)	p_bl_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14108 (R0x371C)	p_bl_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14110 (R0x371E)	p_gb_p4q0	dddd dddd dddd dddd	0 (0x0000)
R14112 (R0x3720)	p_gb_p4q1	dddd dddd dddd dddd	0 (0x0000)
R14114 (R0x3722)	p_gb_p4q2	dddd dddd dddd dddd	0 (0x0000)
R14116 (R0x3724)	p_gb_p4q3	dddd dddd dddd dddd	0 (0x0000)
R14118 (R0x3726)	p_gb_p4q4	dddd dddd dddd dddd	0 (0x0000)
R14208 (R0x3780)	poly_sc_enable	d000 0000 0000 0000	0 (0x0000)
R14210 (R0x3782)	poly_origin_c	0000 0ddd dddd dddd	672 (0x02A0)
R14212 (R0x3784)	poly_origin_r	0000 00dd dddd dddd	424 (0x01A8)

Table 1: Manufacturer-Specific Register List

1 = read-only, always 1; 0 = read-only, always 0; d = programmable; ? = read-only, dynamic

Register Dec(Hex)	Name	Data Format (Binary)	Default Value Dec(Hex)
R14272 (R0x37C0)	p_gr_q5	dddd dddd dddd dddd	0 (0x0000)
R14274 (R0x37C2)	p_rd_q5	dddd dddd dddd dddd	0 (0x0000)
R14276 (R0x37C4)	p_bl_q5	dddd dddd dddd dddd	0 (0x0000)
R14278 (R0x37C6)	p_gb_q5	dddd dddd dddd dddd	0 (0x0000)

Manufacturer Specific Register Descriptions

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12288 R0x3000	15:0	0x0151	chip_version_reg (R/W)	N	N
	Model ID. Read-only. Can be made read/write by clearing R0x301A-B[3].				
R12290 R0x3002	15:0	0x0040	y_addr_start (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.				
R12292 R0x3004	15:0	0x0012	x_addr_start (R/W)	Y	N
	The first column of visible pixels to be read out (not counting any dark columns that may be read). To move the image window, set this register to the starting X value.				
R12294 R0x3006	15:0	0x0317	y_addr_end (R/W)	Y	YM
	The last row of visible pixels to be read out.				
R12296 R0x3008	15:0	0x0519	x_addr_end (R/W)	Y	N
	The last column of visible pixels to be read out.				
R12298 R0x300A	15:0	0x02EE	frame_length_lines (R/W)	Y	YM
	The number of complete lines (rows) in the frame timing. This includes visible lines and vertical blanking lines.				
R12300 R0x300C	15:0	0x0672	line_length_pck (R/W)	Y	YM
	The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time.				
R12302 R0x300E	7:0	0x00	revision_number (R/W)	N	N
R12304 R0x3010	15:0	0xBEEF	lock_control (R/W)	N	N
	This register protects the mirror mode select (register read mode). When set to value 0xBEEF, the horizontal and vertical mirror modes can be changed, otherwise these values are locked.				
R12306 R0x3012	15:0	0x0010	coarse_integration_time (R/W)	Y	N
	Integration time specified in multiples of line_length_pck_.				
R12308 R0x3014	15:0	0x0000	fine_integration_time (R/W)	Y	N
	Fine integration is used to delay the shutter operation after the sample operation is finished. Thus, the integration time is decreased. The resolution is 1 pixel clock time. Note that for short line length (R0x300C, R0x303E) values, the available time for fine shutter is limited. If programmed for more than available time, the normal sensor operation will be disrupted.				
R12310 R0x3016	15:0	0x0010	coarse_integration_time_cb (R/W)	N	N
	Coarse integration time in context B.				
R12312 R0x3018	15:0	0x0000	fine_integration_time_cb (R/W)	N	N
	Fine integration time in context B.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12314 R0x301A	15:0	0x0058	reset_register (R/W)	N	Y
	15	0x0000	grouped_parameter_hold 0 = Update of many of the registers is synchronized to frame start. 1 = Inhibit register updates; register changes will remain pending until this bit is returned to 0. When this bit is returned to 0, all pending register updates will be made on the next frame start.	N	N
	14:13	X	Reserved		
	12	0x0000	smia_serialiser_dis 0: HiSPi Interface Enabled. 1: HiSPi interface Disabled.	N	N
	11	0x0000	forced_pll_on 0: PLL will be powered down when the sensor is in standby (low power mode). 1: PLL will be enabled even when the sensor is in standby.	N	N
	10	0x0000	restart_bad 1: A restart is forced any time a bad frame is detected. This can shorten the delay when waiting for a good frame, since the delay for masking out a bad frame will be the integration time rather than the full-frame time.	N	N
	9	0x0000	mask_bad 0: The sensor will produce bad (corrupted) frames as a result of some register changes. 1: Bad (corrupted) frames are masked within the sensor by extending the vertical blanking time for the duration of the bad frame. Only bad frames caused by the mirror_row register bit will be masked using this feature.	N	N
	8	0x0000	gpi_en 0: The primary input buffers associated with the OUTPUT_ENABLE_N, TRIGGER and STANDBY inputs are powered down and cannot be used. 1: The input buffers are enabled and can be read through R0x3026-7.	N	N
	7	0x0000	parallel_en 0: The parallel data interface (DOUT[15:0], LINE_VALID, FRAME_VALID, and PIXCLK) is disabled and the outputs are placed in a high-impedance state. 1: The parallel data interface is enabled. The output signals can be switched between a driven and a high-impedance state using output-enable control.	N	N

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
	6	0x0001	drive_pins 0: The parallel data interface (DOUT[15:0], LINE_VALID, FRAME_VALID, and PIXCLK) may enter a high-impedance state (depending upon the enabling and use of the pad OUTPUT_ENABLE_N) 1: The parallel data interface is driven. This bit is “do not care” unless bit[7]=1.	N	N
	5	0x0000	reg_rd_en Enable signal to allow read from fuse ID registers.	N	N
	4	0x0001	stdby_eof 0 = Transition to standby is synchronized to the end of a sensor row readout (held-off until LINE_VALID has fallen). 1 = Transition to standby is synchronized to the end of a frame.	N	Y
	3	0x0001	lock_reg Many parameter limitation registers that are specified as read-only are actually implemented as read/write registers. Clearing this bit allows such registers to be written.	N	N
	2	0x0000	stream Setting this bit places the sensor in streaming mode. Clearing this bit places the sensor in a low power mode. The result of clearing this bit depends upon the operating mode of the sensor. Entry and exit from streaming mode can also be controlled from the signal interface.	Y	N
	1	0x0000	restart This bit always reads as 0. Setting this bit causes the sensor to truncate the current frame at the end of the current row and start resetting (integrating) the first row. The delay before the first valid frame is read out is equal to the integration time.	N	Y
	0	0x0000	reset This bit always reads as 0. Setting this bit initiates a reset sequence: the frame being generated will be truncated.	N	Y
	Controls the operation of the sensor. For details see the bit field descriptions.				
R12316 R0x301C	7:0	0x00	mode_select_ (R/W)	Y	N
	This bit is an alias of R0x301A-B[2].				
R12317 R0x301D	7:0	0x00	image_orientation_ (R/W)	Y	YM
	7:2	X	Reserved		
	1	0x00	vert_flip This bit is an alias of R0x3040[15].	Y	YM
	0	0x00	horiz_mirror This bit is an alias of R0x3040[14].	Y	YM
R12318 R0x301E	15:0	0x00A8	data_pedestal (R/W)	N	Y
	Constant offset that is added to pixel values at the end of data path (after all corrections).				
R12321 R0x3021	7:0	0x00	software_reset_ (R/W)	N	Y
	This bit is an alias of R0x301A-B[0].				
R12322 R0x3022	7:0	0x00	grouped_parameter_hold_ (R/W)	Y	N
	This bit is an alias of R0x301A-B[15].				
R12323 R0x3023	7:0	0x00	mask_corrupted_frames_ (R/W)	Y	N
	This bit is an alias of R0x301A-B[9].				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12324 R0x3024	7:0	0x00	pixel_order_ (RO)	Y	N
	This register is a read-only alias of R0x3040[15:14].				
R12326 R0x3026	15:0	0x6500	gpi_status (RO)	N	N
	15:13	0x0003	Reserved		
	12:10	0x0001	Reserved		
	9:7	0x0002	Reserved		
	6:4	0x0000	Reserved		
	3	RO	standby Read-only. Return the current state of the STANDBY input pin. Invalid if R0x301A-B[8]=0.	N	N
	2	RO	trigger Read-only. Return the current state of the TRIGGER input pin. Invalid if R0x301A-B[8]=0.	N	N
	1	RO	oe_n Read-only. Return the current state of the OUTPUT_ENABLE_N input pin. Invalid if R0x301A-B[8]=0.	N	N
	0	RO	saddr Read-only. Return the current state of the pin SADDR input pin. This pad is not controlled by gpi_en.	N	N
	Reflects the status of the input pins: STANDBY(3), TRIGGER(2), OUTPUT_ENABLE_N(1), SADDR(0). Upper bits are hardwired to a constant.				
R12328 R0x3028	15:0	0x0010	row_speed (R/W)	N	N
	Bits [6:4] of this register define the phase of the output PIXCLK 2 sets of values are correct: a) 000, 010, 100, 110 => 0 delay (rising edge of PIXCLK coincides DOUT change). b) 001, 011, 101, 111 => 1/2 clk delay (falling edge of PIXCLK coincides DOUT change).				
R12330 R0x302A	15:0	0x0006	vt_pix_clk_div (R/W)	N	N
	Sets the ratio of the serial output clock and sensor operation clock (P2 clock divider in PLL).				
R12332 R0x302C	15:0	0x0001	vt_sys_clk_div (R/W)	N	N
	Sets the ratio of the VCO clk and the serial output clock (P1 divider in PLL).				
R12334 R0x302E	15:0	0x0004	pre_pll_clk_div (R/W)	N	N
	Clock divisor applied to EXTCLK to generate PLL input clock. Shows the n+1 value.				
R12336 R0x3030	15:0	0x0042	pll_multiplier (R/W)	N	N
	Clock multiplier applied to PLL input clock.				
R12342 R0x3036	15:0	0x000C	op_pix_clk_div (R/W)	N	Y
	Clock divisor applied to the output system clock to generate the output pixel clock.				
R12344 R0x3038	15:0	0x0002	op_sys_clk_div (R/W)	N	Y
	Clock divisor applied to PLL output clock to generate output system clock.				
R12346 R0x303A	15:0	0xFFFF	frame_count (RO)	N	N
	Counts the number of processed frames. At the startup is initialized to 0xFFFF.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12348 R0x303C	15:0	0x0000	frame_status (RO)	N	N
	15:4	X	Reserved		
	3	RO	frame_status_pll_locked Reflects the status of the pll_locked pin from the PLL.	N	N
	2	RO	frame_status_frame_start_during_gph Signifies that a new frame has started while group parameter hold is high. This tells the user if the sensor frame-sync start event has been missed, and therefore gains/integration time changes are going to take effect delayed by 1 frame.	N	N
	1	RO	standby_status This bit indicates that the sensor is in standby state. It can be polled after standby is entered to see when the real low-power state is entered; which can happen at the end of row or frame depending on bit R0x301A[4].	N	N
	0	RO	framesync Set on register write and reset on frame synchronization. Acts as debug flag to verify that register writes completed before last frame synchronization.	N	N
R12350 R0x303E	15:0	0x0672	line_length_pck_cb (R/W)	Y	N
	Line length in context B. The number of pixel clock periods in one line (row) time. This includes visible pixels and horizontal blanking time. For smooth operation this should be the same value as LINE_LENGTH_PCK (0x300C).				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12352 R0x3040	15:0	0x0000	read_mode (R/W)	Y	YM
	15	0x0000	vert_flip 0: Normal readout 1: Readout is flipped (mirrored) vertically so that the row specified by y_addr_end_ (+1) is read out of the sensor first. Changing this register can only be done when streaming is disabled	Y	YM
	14	0x0000	horiz_mirror 0: Normal readout 1: Readout is mirrored horizontally so that the column specified by x_addr_end_ (+1) is read out of the sensor first. Changing this register can only be done when streaming is disabled	Y	YM
	13	0x0000	read_mode_col_bin Column binning mode in context A. Pixel values are averaged in the digital domain. Use when skipping is enabled by setting x_odd_inc.	Y	N
	12	0x0000	read_mode_row_bin Analog row binning control in context A. Use when row-wise skipping is enabled by setting y_odd_inc. The y_addr_start must be an even number when using row binning.	Y	N
	11	0x0000	read_mode_col_bin_cb Column binning mode in context B. Pixel values are averaged in the digital domain. Use when skipping is enabled by setting x_odd_inc_cb.	Y	N
	10	0x0000	read_mode_row_bin_cb Analog row binning control for context B. Use when row-wise skipping is enabled by setting y_odd_inc_cb. The y_addr_start_cb must be an even number when using row binning.	Y	N
	9:7	X	Reserved		
	6	0x0000	read_mode_samp_sum Switch between multiple sample averaging and summing.	Y	N
	5	0x0000	read_mode_col_sum Column sum mode. Pixel values are summed in the digital domain. Use when skipping is enabled by setting x_odd_inc.	Y	N
	4	0x0000	read_mode_alu_bin When set, the binned rows will be sampled and converted separately and added in ADC ALU. Compare with source follower bin mode. Note that in this mode, the minimum line length pck might be a bigger value.	N	N
	3:0	X	Reserved		
R12354 R0x3042	15:0	0x0000	extra_delay (R/W)	Y	N
	The last row in the frame is extended by the number of the sensor core clock periods specified here. This register can be used to fine-tune the sensor maximum frame-rate.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12358 R0x3046	15:0	0x0000	flash (R/W)	Y	Y
	15	RO	strobe Reflects the current state of the FLASH output signal. Read-only.	N	N
	14	RO	triggered Indicates that the FLASH output signal was asserted for the current frame. Read-only.	N	N
	13:9	X	Reserved		
	8	0x0000	en_flash Enables the flash. The flash is asserted when an integration is ongoing.	Y	Y
	7	0x0000	invert_flash Invert flash output signal. When set, the FLASH output signal will be active low.	N	N
	6	X	Reserved		
	5:3	0x0000	xenon_frames_enable 0: Xenon flash disabled. 1-6: Number of frames with Xenon flash. 7: Xenon flash enable for all frames.	N	N
	2:0	0x0000	xenon_frames_delay XENON_FRAMES_DELAY[2:0]: Number of the frames before the first time Xenon flash is actuated.	Y	N
	See bit fields for definition of flash and Xenon Flash control.				
R12360 R0x3048	15:0	0x0100	flash2 (R/W)	N	N
	Xenon flash pulse width in clock periods.				
R12374 R0x3056	15:0	0x0080	green1_gain (R/W)	Y	N
	Digital gain for Green1 (Gr) pixels in Context A, in format of xxxx.yyyyyyy.				
R12376 R0x3058	15:0	0x0080	blue_gain (R/W)	Y	N
	Digital gain for Blue pixels in Context A, in format of xxxx.yyyyyyy.				
R12378 R0x305A	15:0	0x0080	red_gain (R/W)	Y	N
	Digital gain for Red pixels in Context A, in format of xxxx.yyyyyyy.				
R12380 R0x305C	15:0	0x0080	green2_gain (R/W)	Y	N
	Digital gain for Green2 (Gb) pixels in Context A, in format of xxxx.yyyyyyy.				
R12382 R0x305E	15:0	0x0080	global_gain (R/W)	Y	N
	Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers in context A. Reading from this register returns the value most recently written to the green1_gain register.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12384 R0x3060	15:0	0x0000	analog_gain (R/W)	Y	N
	15	0x0000	gain_test_enable Enables gain test mode. The coarse gain will be replaced with a counter that is incremented every 4 rows, so the pattern repeats every 32 rows. The fine gain pattern is a 4 bit walking 1and steps up every 32 rows. The pattern repeats every 160 rows. The fine gain pattern is OR'd with the fine gain registry setting when enabled.	N	N
	14:12	0x0000	coarse_gain_cb Coarse Analog gain in context B. See Coarse gain context A description for limits.	Y	N
	11:8	0x0000	fine_gain_cb Fine analog gain in context B	Y	N
	7	X	Reserved		
	6:4	0x0000	coarse_gain Coarse Analog gain in context A. The gain is 2^value with the maximum value being 8x. A value of 3 therefore gives 8x gain. In SDR mode the system is only capable of supporting a coarse gain of up to 12x gain where coarse gain and fine gain are used to achieve 12x (8x from coarse gain, 4x from fine gain)	Y	N
	3:0	0x0000	fine_gain Fine analog gain in context A. This is a fractional gain and the gain is value/16.	Y	N
	Defines analog gains for both contexts. Maximum supported gain is 12x (8x from coarse gain, 4x from fine gain)				
R12388 R0x3064	15:0	0x1982	smia_test (R/W)	N	N
	15:13	X	Reserved		
	12	0x0001	Reserved		
	11:10	0x0002	Reserved		
	9	0x0000	Reserved		
	8	0x0001	embedded_data 0: Frames out of the sensor exclude the embedded data. 1: Frames of data out of the sensor include 2 rows of embedded data. This register field should only be change while the sensor is in software standby. Disabling the embedded data will not reduce the number of vertical blanking rows.	N	N
	7	0x0001	embedded_stats_en 0: Embedded statistics is not transmitted on the 2 stats rows after the frame pixel data. 1: Embedded statistics is transmitted on the 2 stats data rows after the frame pixel data.	N	N
	6:4	X	Reserved		
	3:0	0x0002	Reserved		

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12398 R0x306E	15:0	0x9010	datapath_select (R/W)	N	N
	15:13	0x0004	slew_rate_ctrl_parallel Selects the slew (edge) rate for the DOUT[15:0], FRAME_VALID, LINE_VALID and FLASH outputs. Only affects the FLASH output when parallel data output is disabled. The value 7 results in the fastest edge rates on these signals. Slowing down the edge rate can reduce ringing and electro-magnetic emissions.	N	N
	12:10	0x0004	slew_rate_ctrl_pixclk Selects the slew (edge) rate for the PIXCLK output. Has no effect when parallel data output is disabled. The value 7 results in the fastest edge rates on this signal. Slowing down the edge rate can reduce ringing and electromagnetic emissions.	N	N
	9	0x0000	high_vcm 0: For SLVS low vcm for the HiSPi Interface. VDD_SLVS must be 0.4V 1: For sub-SLVS high vcm. VDD_SLVS = VDDIO = 1.8V	N	N
	8	0x0000	datapath_select_bit8 Not used.	N	N
	7:5	X	Reserved		
	4	0x0001	Reserved		
	3:2	X	Reserved		
	1:0	0x0000	special_line_valid 00: Normal behavior of LINE_VALID 01: LINE_VALID is driven continuously (continue generating LINE_VALID during vertical blanking) 10: LINE_VALID is driven continuously as LINE_VALID XOR FRAME_VALID 11: Reserved.	N	N
R12400 R0x3070	15:0	0x0000	test_pattern_mode (R/W)	N	Y
	0: Normal operation. Generate output data from pixel array 1: Solid color test pattern. 2: Full color bar test pattern 3: Fade to gray color bar test pattern 256: Walking 1s test pattern (12-bit) 512: Walking 1s test pattern (16-bits Other: Reserved.				
R12402 R0x3072	15:0	0x0000	test_data_red (R/W)	N	Y
	The value for red pixels in the Bayer data used for the solid color test pattern and the test cursors.				
R12404 R0x3074	15:0	0x0000	test_data_greenr (R/W)	N	Y
	The value for green pixels in red/green rows of the Bayer data used for the solid color test pattern and the test cursors.				
R12406 R0x3076	15:0	0x0000	test_data_blue (R/W)	N	Y
	The value for blue pixels in the Bayer data used for the solid color test pattern and the test cursors.				
R12408 R0x3078	15:0	0x0000	test_data_greenb (R/W)	N	Y
	The value for green pixels in blue/green rows of the Bayer data used for the solid color test pattern and the test cursors.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12410 R0x307A	15:0	0x0000	test_raw_mode (R/W)	N	N
	15:2	X	Reserved		
	1	0x0000	Reserved		
	0	0x0000	Reserved		
R12422 R0x3086	15:0	0x0000	seq_data_port (R/W)	N	N
	Register used to write to or read from the sequencer RAM.				
R12424 R0x3088	15:0	0xC000	seq_ctrl_port (R/W)	N	N
	15	RO	sequencer_stopped Showing that sequencer is stopped (STANDBY mode) and the RAM is available for read or write.	N	N
	14	0x0001	auto_inc_on_read If 1 => The access_address is incremented (by 1) after each read operation from seq_data_port (which returns only1 byte)	N	N
	13:10	X	Reserved		
	9:0	0x0000	access_address When in STANDBY (not streaming) mode: address pointer to the sequencer RAM.	N	N
	Register controlling the read and write to sequencer RAM.				
R12426 R0x308A	15:0	0x0012	x_addr_start_cb (R/W)	N	N
	X_ADDR_START for context B				
R12428 R0x308C	15:0	0x0040	y_addr_start_cb (R/W)	N	N
	Y_ADDR_START for context B				
R12430 R0x308E	15:0	0x0519	x_addr_end_cb (R/W)	N	N
	X_ADDR_END for context B				
R12432 R0x3090	15:0	0x0317	y_addr_end_cb (R/W)	N	N
	Y_ADDR_END for context B				
R12448 R0x30A0	15:0	0x0001	x_even_inc (RO)	N	N
	Read-only.				
R12450 R0x30A2	15:0	0x0001	x_odd_inc (R/W)	Y	YM
	1: No skip. 3: Skip 2. Other values are not supported.				
R12452 R0x30A4	15:0	0x0001	y_even_inc (RO)	N	N
	Read-only.				
R12454 R0x30A6	15:0	0x0001	y_odd_inc (R/W)	Y	YM
	1: No skip. 3: Skip 2. Other values are not supported.				
R12456 R0x30A8	15:0	0x0001	y_odd_inc_cb (R/W)	Y	YM
	Y_ODD_INC context B				
R12458 R0x30AA	15:0	0x02EE	frame_length_lines_cb (R/W)	Y	YM
	FRAME_LENGTH_LINES context B. See description for R0x300A				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12462 R0x30AE	15:0	0x0001	x_odd_inc_cb (R/W)	Y	YM
	X_ODD_INC context B				
R12464 R0x30B0	15:0	0x0000	digital_test (R/W)	N	Y
	15	X	Reserved		
	14	0x0000	pll_complete_bypass 0: PLL is enabled 1: PLL is bypassed. EXTCLK will be used. Note that the serial interface does not function when PLL is bypassed.	N	N
	13	0x0000	context_b Context Control. 0: Use Context A 1: Use Context B	Y	N
	12:8	X	Reserved		
	7	0x0000	mono_chrome_operation Mono Chrome Sensor Operation. 0: Normal operation. 1: Sensor will operate similar to a mono chrome sensor. Useful in the bin2 mode.	Y	N
	6:5	X	Reserved		
	4:2	0x0000	samp_nr Shows the number of sample (minus 1) for each row. As an example, if set to 1, each row will be sampled 2 times and added in the ADC ALU. The maximum value is 7 that corresponds to 8 samples. Note that multiple sampling increases the minimum required line length pck. The purpose is to reduce the noise.	N	N
	1	X	Reserved		
	0	0x0000	tx_latch_mode When set, the logic operates in Tx latch mode. The pixels that are not under integration / exposure are connected by activated Tx transistor to VAA.	N	N
R12466 R0x30B2	15:0	0x0000	tempsens_data (R/W)		
	Output value from temperature sensor.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12468 R0x30B4	15:0	0x0000	tempsens_ctrl (R/W)	N	N
	15:6	0x0000	retrigger_threshold When the measured absolute temperature (ADC value) changes more than this setting, the delta dark algorithm is retriggered and the temperature is saved as the comparison level for the following measurement. If the value is set to zero, the retrigger function will be disabled.	N	N
	5	0x0000	temp_clear_value Clear data register (sanity check).	N	N
	4	0x0000	temp_start_conversion When asserted, a new temp value will be generated for each frame capture. When asserted in standby mode, a new temp value will be generated.	N	N
	3:1	0x0000	Reserved		
	0	0x0000	tempsens_power_on tempsens_power_on	N	N
	Control register for temperature sensor				
R12470 R0x30B6	15:0	0x0000	spare_0x30b6 (R/W)		
	Spare register for tempsens calibration values.				
R12472 R0x30B8	15:0	0x0000	spare_0x30b8 (R/W)	N	N
	Spare register for tempsens calibration data.				
R12474 R0x30BA	15:0	0x002C	digital_ctrl (R/W)	Y	N
	15:9	X	Reserved		
	8	0x0000	Reserved		
	7:6	X	Reserved		
	5	0x0001	dither_enable Enables dithering after digital gain. Will have no effect on data when the digital gain is set to 1.	N	N
	4	X	Reserved		
	3:2	0x0003	Reserved		
	1:0	0x0000	Reserved		
R12476 R0x30BC	15:0	0x0080	green1_gain_cb (R/W)	Y	N
	Digital gain for Green1 (Gr) pixels in Context B, in format of xxxx.yyyyyyy.				
R12478 R0x30BE	15:0	0x0080	blue_gain_cb (R/W)	Y	N
	Digital gain for Blue pixels in Context B, in format of xxxx.yyyyyyy.				
R12480 R0x30C0	15:0	0x0080	red_gain_cb (R/W)	Y	N
	Digital gain for Red pixels in Context B, in format of xxxx.yyyyyyy.				
R12482 R0x30C2	15:0	0x0080	green2_gain_cb (R/W)		
	Digital gain for Green2 (Gb) pixels in Context B, in format of xxxx.yyyyyyy.				
R12484 R0x30C4	15:0	0x0080	global_gain_cb (R/W)	Y	N
	Writing a gain to this register is equivalent to writing that code to each of the 4 color-specific gain registers in Context B. Reading from this register returns the value most recently written to the green1_gain_cb register.				
R12486 R0x30C6	15:0	0x0123	tempsens_calib1 (R/W)	N	N
	Register to store tempsens calibration value.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12488 R0x30C8	15:0	0x4567	tempsens_calib2 (R/W)	N	N
	Register to store tempsens calibration value.				
R12490 R0x30CA	15:0	0x89AB	tempsens_calib3 (R/W)	N	N
	Register to store tempsens calibration value.				
R12492 R0x30CC	15:0	0xCDEF	tempsens_calib4 (R/W)	N	N
	Register to store tempsens calibration value.				
R12494 R0x30CE	15:0	0x0000	grr_control1 (R/W)	N	N
	15:9	X	Reserved		
	8	0x0000	slave_sh_sync_mode Also called SURROUND VIEW mode. When set and the sensor is set to stream mode, it waits for an external trigger signal. When a trigger is received, a time interval of frame length lines is started. The shutter pointers are started at appropriate point and when this time interval is finished, the read out is started. The external trigger period must not be less than frame length lines, otherwise the triggers happening during the time interval will be ignored.	N	N
	7	0x0000	shutter_always_open When set to 1, the shutter pin will always be asserted (OPEN) in GRR mode.	N	N
	6	0x0000	shutter_disable When set to 1, the shutter pin will be disabled (CLOSED) in GRR mode.	N	N
	5	0x0000	frame_start_mode This bit controls the frame timing of the first frame when entering stream mode (or trigger mode). When low, the integration time is started and then readout begins. It means that the first frame will start after a delay equal to CIT. When high, a frame time is started and at the appropriate time point, the integration starts. It means that the first frame will start after one frame time.	N	N
	4	0x0000	slave_mode When set to 1, the sensor readout start will be synchronized with the external trigger (applied to pad TRIGGER).	N	N
	3	X	Reserved		
	2	0x0000	Reserved		
	1	X	Reserved		
	0	0x0000	grr_mode 0: Normal ERS mode. 1: Global reset release mode.	N	N
R12496 R0x30D0	15:0	0x0005	grr_control2 (R/W)	N	N
	15:8	X	Reserved		
	7:0	0x0005	gr_delay Delay between external trigger and global reset in number of rows.	N	N

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12498 R0x30D2	15:0	0x0004	grr_control3 (R/W)	N	N
	15:0	0x0004	ext_shut_pulse_width Width of the external shutter pulse in clock cycles. When set to zero, the shutter pulse will be controlled by GRR_CONTROL4.	N	N
R12506 R0x30DA	15:0	0x000A	grr_control4 (R/W)		
	15:0	0x000A	ext_shut_delay	N	N
	Delay between external trigger and close of external shutter in number of rows.				
R12544 R0x3100	15:0	0x0000	aectrlreg (R/W)	Y	N
	15:8	X	Reserved		
	7	0x0000	dcg_manual_set_cb Manual DCG value used in context B.	Y	N
	6:3	X	Reserved		
	2	0x0000	dcg_manual_set This bit is used to decide the DCG gain in context A. 1: High gain. 0: Low gain.	Y	N
	1:0	X	Reserved		
R12608 R0x3140	15:0	0x0000	ae_roi_x_start_offset (R/W)		
	Number of pixels into each row before the ROI starts NOTE: if statistics are being gathered from a scaled image then the 'number of pixels' value must be the number of scaled pixels				
R12610 R0x3142	15:0	0x0000	ae_roi_y_start_offset (R/W)	N	N
	Number of rows into each frame before the ROI starts				
R12612 R0x3144	15:0	0x0508	ae_roi_x_size (R/W)		
	Number of columns in the ROI				
R12614 R0x3146	15:0	0x02D8	ae_roi_y_size (R/W)		
	Number of rows in the ROI				
R12616 R0x3148	15:0	0x0290	ae_hist_begin_perc (R/W)	N	N
	Defines the percentage of Gr pixels that must have values below hist_begin. Specified as a number < 1 = 0.xx...xx				
R12618 R0x314A	15:0	0xFFF8	ae_hist_end_perc (R/W)		
	Defines the percentage of Gr pixels that must have values below hist_end. Specified as a number < 1 = 0.xx...xx. A value of all 1s is treated as a special case and equates to 1.0 (100%)				
R12620 R0x314C	15:0	0x0100	ae_hist_div (R/W)		
	Defines the point at which the histogram is divided into the low and high end. Boundary value = hist_div*16				
R12622 R0x314E	15:0	0x0020	ae_norm_width_min (R/W)		
	Defines the minimum histogram width normalization factor (=norm_width_min*16), for norm_abs_dev calculation. A value of all 1s turns off the norm_width_min option, i.e. all absolute deviation is normalized by hist_end - hist_begin				
R12624 R0x3150	15:0	0x0000	ae_mean_h (RO)		
	The true mean of all Gr pixels in the ROI (higher bits)				
R12626 R0x3152	15:0	0x0000	ae_mean_l (RO)		
	The true mean of all Gr pixels in the ROI (16 least significant bits)				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12628 R0x3154	15:0	0x0000	ae_hist_begin_h (RO)		
	Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (higher bits)				
R12630 R0x3156	15:0	0x0000	ae_hist_begin_l (RO)	N	N
	Code value corresponding to the histogram bin below which (hist_begin_perc*100)% of pixels exist (lower 16 bits)				
R12632 R0x3158	15:0	0x0000	ae_hist_end_h (RO)	N	N
	Code value corresponding to the histogram bin below which (hist_end_perc*100)% of pixels exist (higher bits)				
R12634 R0x315A	15:0	0x0000	ae_hist_end_l (RO)	N	N
	Code value corresponding to the histogram bin below which (hist_end_perc*100)% of pixels exist (lower 16 bits)				
R12636 R0x315C	15:0	0x0000	ae_low_end_mean_h (RO)	N	N
	The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div) (higher bits)				
R12638 R0x315E	15:0	0x0000	ae_low_end_mean_l (RO)	N	N
	The true mean of all Gr pixels in the ROI that fall into the low end of the histogram (where low end is defined by hist_div) (lower 16 bits)				
R12640 R0x3160	15:0	0x0000	ae_perc_low_end (RO)		
	Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx				
R12642 R0x3162	15:0	0x0000	ae_norm_abs_dev (RO)		
	Percentage of Gr pixels in ROI that fall into the low end of the histogram. Specified as a number < 1 = 0.xx...xxx				
R12716 R0x31AC	15:0	0x0C0C	data_format_bits (R/W)		
	15:13	X	Reserved		
	12:8	0x000C	data_format_in The bit-width of the pixel data pre compression or truncation	N	N
	7:5	X	Reserved		
	4:0	0x000C	data_format_out The bit-width of the pixel data post compression or truncation. 0x0C: 12-bit 0x0A: 10-bit	N	N
	Data formats pre and post compression or truncation. Compression or truncation is selected in COMPANDING 0x31D0				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12718 R0x31AE	15:0	0x0304	serial_format (R/W)	N	N
	15:10	X	Reserved		
	9:8	0x0003	serial_format_type When the serial interface is enabled (reset_register[12]=0), this register controls which serial interface type is in use. 3 for HISPI is valid.	N	N
	7:3	X	Reserved		
	2:0	0x0004	serial_format_lanes Configures the number of lanes to be used: 4: Quad-lane HiSPi 3: Three lane HiSPi 2: Dual-lane HiSPi 1: Single-lane HiSPi or for Parallel	N	N
	When the serial interface is enabled (reset_register[12]=0), this register controls which serial interface is in use. Any non-zero serial_format_descriptor value is a legal value for this register. The upper byte of this register (interface type) is read-only. The lower byte configures the number of HiSPi lanes to be used: 4: Quad-lane HiSPi 3: Three lane HiSPi 2: Dual-lane HiSPi 1: Single-lane HiSPi				
R12736 R0x31C0	15:0	0x8000	hispi_timing (R/W)		
	15	0x0001	reva_comp 0: 'Disabled' - lowest power state,*_mode_sel = 2'b00. This is the 'power up' state and the state when the sensor goes into standby. - 'Inactive' - *_mode_sel = 2'b11 but internal high speed clocks gated and transmitted clock can be stopped (as selected by 'cont_tx_clk'). This is the state during blanking - 'Active' - *_mode_sel - high speed transmission mode 1: HiSPi protocol operates as in previous designs, i.e. *_mode_sel will always = 2'b11. When the sensor goes into standby the HiSPi data and clock lanes will go hi-Z (by asserting*_zstate)	N	N
	14:12	0x0000	clock_del Delay applied to the clock lane in 1/8 unit interval (UI) steps.	N	N
	11:9	0x0000	data3_del Delay applied to Data Lane 3 in 1/8 unit interval (UI) steps.	N	N
	8:6	0x0000	data2_del Delay applied to Data Lane 2 in 1/8 unit interval (UI) steps.	N	N
	5:3	0x0000	data1_del Delay applied to Data Lane 1 in 1/8 unit interval (UI) steps.	N	N
	2:0	0x0000	data0_del Delay applied to Data Lane 0 in 1/8 unit interval (UI) steps.	N	N
	Within the HiSPi PHY there is a DLL connected to the clock lane and each data lane, which acts as a control master for the output delay buffers. This additional delay allows the user to increase the setup or hold time at the receiver circuits and can be used to compensate for skew introduced in PCB design. If the DLL timing adjustment is not required, the data and clock lane delay settings should be set to a default code of 0x000 to reduce jitter, skew, and power dissipation.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12738 R0x31C2	15:0	0xFFFF	hispi_blanking (R/W)	N	N
	HiSPi Blanking Data				
R12740 R0x31C4	15:0	0xF555	hispi_sync_patt (R/W)	N	N
	15:8	0x00F5	Reserved		
	7:0	0x0055	Reserved		
	HiSPi Sync Pattern				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12742 R0x31C6	15:0	0x8000	hispi_control_status (R/W)	N	N
	15:14	X	Reserved		
	13	0x0000	Reserved		
	12	X	Reserved		
	11:10	0x0000	hispi_mode_sel Will select the HiSPi output protocol: b00 for HiSPi S -Streaming b01 for HiSPi SP -Packetized	N	N
	9	0x0000	Reserved		
	8	0x0000	Reserved		
	7	0x0000	test_enable When asserted, the test pattern is output through the HiSPi PHY interface.	N	N
	6:4	0x0000	test_mode Define test mode to be applied to HiSPi interface if test_en is asserted 0: Transmit 0 on each physical line of all enabled data and clock lanes (reserved if using separate HiSPi PHY 1: Reserved 2: Transmit differential 0 on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 3: Transmit differential 1 on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 4: Transmit a square wave at half the potential serial data rate on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 5: Transmit a square wave at the pixel data rate on all enabled data and clock lanes (data lanes ONLY if using separate HiSPi PHY) 6: Reserved 7: Transmit a continuous repeated sequence of pseudo random data, with no SAV code, copied on all enabled data lanes	N	N
	3	0x0000	blanking_data_enable 0,: The default pattern (constant 1) is output during horizontal and vertical blanking periods 1: the pattern defined by the blanking_data input is output during horizontal and vertical blanking periods Note: For the HiSPi S Streaming	N	N
	2	0x0000	streaming_mode 0,: Data will be transmitted in 'packetized' format when HiSPi SP protocol is selected 1,: Data will be transmitted in 'streaming' format when HiSPi SP protocol is selected Not relevant when hispi_mode_sel[1:0] is not set to 2'	N	N
	1	0x0000	output_msb_first Output MSB first	N	N
	0	0x0000	vert_left_bar_en An optional filler code of 1s may be padded after the sync code. When filler codes are enabled, the receiver must window the received image to eliminate first 4 data words (columns per PHYs).	N	N
	See descriptions in the bit fields.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12744 R0x31C8	15:0	0x0000	hispi_crc_0 (RO)	N	N
R12746 R0x31CA	15:0	0x0000	hispi_crc_1 (RO)	N	N
R12748 R0x31CC	15:0	0x0000	hispi_crc_2 (RO)		
R12750 R0x31CE	15:0	0x0000	hispi_crc_3 (RO)		
R12752 R0x31D0	15:0	0x0001	companding (R/W)		
	15:1	X	Reserved		
	0	0x0001	compand_en Enables companding, or compression the actual compression used is appropriate for the pre and post compression data sizes in DATA_FORMAT_BITS 0x31AC	N	N
R12754 R0x31D2	15:0	0x0000	stat_frame_id (R/W)	N	N
R12758 R0x31D6	15:0	0xFFFF	i2c_wrt_checksum (R/W)		
	Checksum of I^2C write operations.				
R12776 R0x31E8	15:0	0x0000	horizontal_cursor_position (R/W)	N	N
	Specify the start row for the test cursor.				
R12778 R0x31EA	15:0	0x0000	vertical_cursor_position (R/W)	N	N
	Specify the start column for the test cursor.				
R12780 R0x31EC	15:0	0x0000	horizontal_cursor_width (R/W)	N	N
	Specify the width, in rows, of the horizontal test cursor. A width of 0 disables the cursor.				
R12782 R0x31EE	15:0	0x0000	vertical_cursor_width (R/W)	N	N
	Specify the width, in columns, of the vertical test cursor. A width of 0 disables the cursor.				
R12788 R0x31F4	15:0	0x0000	fuse_id1 (R/W)		
	Bits 15:0 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/ Write (the programmed value can be over-written and will be restored on reset)				
R12790 R0x31F6	15:0	0x0000	fuse_id2 (R/W)	N	N
	Bits 31:16 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/ Write (the programmed value can be over-written and will be restored on reset)				
R12792 R0x31F8	15:0	0x0000	fuse_id3 (R/W)		
	Bits 47:32 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/ Write (the programmed value can be over-written and will be restored on reset)				
R12794 R0x31FA	15:0	0x0000	fuse_id4 (R/W)		
	Bits 63:48 of the fused chip ID. Read protected. Set reset_register[5] to get access to register. Before the fuses are programmed, this register will read 0x0000. After programming it will read back the programmed value. Read/ Write (the programmed value can be over-written and will be restored on reset)				
R12796 R0x31FC	15:0	0x3020	cci_ids (R/W)	N	N
	CCI addresses. Can be written only if x301A[3] Lock Reg=0.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12800 R0x3200	15:0	0x0000	adacd_control (R/W)	N	N
	15:2	X	Reserved		
	1	0x0000	adacd_filter_en 0: ADACD Noise Filter is disabled. 1: ADACD Noise Filter is enabled.	N	N
	0	0x0000	low_light Adjust ADACD algorithm for low light	N	N
R12802 R0x3202	15:0	0x008C	adacd_noise_model1 (R/W)	N	N
	Noise coefficient code, which is equal to 256 * noise floor.				
R12806 R0x3206	15:0	0x0403	adacd_noise_floor1 (R/W)	N	N
	15:8	0x0004	noise_floor1_high Used when analog gain is less than adacd_gain_threshold_1 and bigger than adacd_gain_threshold_0.	N	N
	7:0	0x0003	noise_floor1_low Used when analog gain is less than adacd_gain_threshold_0.	N	N
R12808 R0x3208	15:0	0x0A06	adacd_noise_floor2 (R/W)	N	N
	15:8	0x000A	noise_floor2_high Used when analog gain is bigger than adacd_gain_threshold_2.	N	N
	7:0	0x0006	noise_floor2_low Used when analog gain is less than adacd_gain_threshold_2 and bigger than adacd_gain_threshold_1.	N	N
R12810 R0x320A	15:0	0x0080	adacd_pedestal (R/W)	N	N
	Normally must be set to same value as noise pedestal.				
R13824 R0x3600	15:0	0x0000	p_gr_p0q0 (R/W)	N	N
	P0 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13826 R0x3602	15:0	0x0000	p_gr_p0q1 (R/W)	N	N
	P0 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13828 R0x3604	15:0	0x0000	p_gr_p0q2 (R/W)		
	P0 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13830 R0x3606	15:0	0x0000	p_gr_p0q3 (R/W)	N	N
	P0 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13832 R0x3608	15:0	0x0000	p_gr_p0q4 (R/W)		
	P0 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13834 R0x360A	15:0	0x0000	p_rd_p0q0 (R/W)	N	N
	P0 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13836 R0x360C	15:0	0x0000	p_rd_p0q1 (R/W)	N	N
	P0 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R13838 R0x360E	15:0	0x0000	p_rd_p0q2 (R/W)		
	P0 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13840 R0x3610	15:0	0x0000	p_rd_p0q3 (R/W)	N	N
	P0 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13842 R0x3612	15:0	0x0000	p_rd_p0q4 (R/W)	N	N
	P0 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13844 R0x3614	15:0	0x0000	p_bl_p0q0 (R/W)	N	N
	P0 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13846 R0x3616	15:0	0x0000	p_bl_p0q1 (R/W)	N	N
	P0 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13848 R0x3618	15:0	0x0000	p_bl_p0q2 (R/W)	N	N
	P0 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13850 R0x361A	15:0	0x0000	p_bl_p0q3 (R/W)	N	N
	P0 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13852 R0x361C	15:0	0x0000	p_bl_p0q4 (R/W)	N	N
	P0 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13854 R0x361E	15:0	0x0000	p_gb_p0q0 (R/W)	N	N
	P0 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13856 R0x3620	15:0	0x0000	p_gb_p0q1 (R/W)	N	N
	P0 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13858 R0x3622	15:0	0x0000	p_gb_p0q2 (R/W)		
	P0 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13860 R0x3624	15:0	0x0000	p_gb_p0q3 (R/W)		
	P0 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13862 R0x3626	15:0	0x0000	p_gb_p0q4 (R/W)		
	P0 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13888 R0x3640	15:0	0x0000	p_gr_p1q0 (R/W)		
	P1 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				

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R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R13890 R0x3642	15:0	0x0000	p_gr_p1q1 (R/W)		
	P1 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13892 R0x3644	15:0	0x0000	p_gr_p1q2 (R/W)		
	P1 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13894 R0x3646	15:0	0x0000	p_gr_p1q3 (R/W)		
	P1 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13896 R0x3648	15:0	0x0000	p_gr_p1q4 (R/W)		
	P1 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13898 R0x364A	15:0	0x0000	p_rd_p1q0 (R/W)		
	P1 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13900 R0x364C	15:0	0x0000	p_rd_p1q1 (R/W)		
	P1 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13902 R0x364E	15:0	0x0000	p_rd_p1q2 (R/W)		
	P1 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13904 R0x3650	15:0	0x0000	p_rd_p1q3 (R/W)		
	P1 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13906 R0x3652	15:0	0x0000	p_rd_p1q4 (R/W)	N	N
	P1 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13908 R0x3654	15:0	0x0000	p_bl_p1q0 (R/W)		
	P1 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13910 R0x3656	15:0	0x0000	p_bl_p1q1 (R/W)	N	N
	P1 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13912 R0x3658	15:0	0x0000	p_bl_p1q2 (R/W)	N	N
	P1 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13914 R0x365A	15:0	0x0000	p_bl_p1q3 (R/W)	N	N
	P1 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13916 R0x365C	15:0	0x0000	p_bl_p1q4 (R/W)	N	N
	P1 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				

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R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R13918 R0x365E	15:0	0x0000	p_gb_p1q0 (R/W)	N	N
	P1 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13920 R0x3660	15:0	0x0000	p_gb_p1q1 (R/W)	N	N
	P1 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13922 R0x3662	15:0	0x0000	p_gb_p1q2 (R/W)	N	N
	P1 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13924 R0x3664	15:0	0x0000	p_gb_p1q3 (R/W)	N	N
	P1 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13926 R0x3666	15:0	0x0000	p_gb_p1q4 (R/W)	N	N
	P1 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13952 R0x3680	15:0	0x0000	p_gr_p2q0 (R/W)	N	N
	P2 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13954 R0x3682	15:0	0x0000	p_gr_p2q1 (R/W)	N	N
	P2 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13956 R0x3684	15:0	0x0000	p_gr_p2q2 (R/W)	N	N
	P2 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13958 R0x3686	15:0	0x0000	p_gr_p2q3 (R/W)	N	N
	P2 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13960 R0x3688	15:0	0x0000	p_gr_p2q4 (R/W)	N	N
	P2 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R13962 R0x368A	15:0	0x0000	p_rd_p2q0 (R/W)	N	N
	P2 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13964 R0x368C	15:0	0x0000	p_rd_p2q1 (R/W)	N	N
	P2 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13966 R0x368E	15:0	0x0000	p_rd_p2q2 (R/W)	N	N
	P2 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13968 R0x3690	15:0	0x0000	p_rd_p2q3 (R/W)	N	N
	P2 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				

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R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R13970 R0x3692	15:0	0x0000	p_rd_p2q4 (R/W)	N	N
	P2 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R13972 R0x3694	15:0	0x0000	p_bl_p2q0 (R/W)	N	N
	P2 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13974 R0x3696	15:0	0x0000	p_bl_p2q1 (R/W)	N	N
	P2 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13976 R0x3698	15:0	0x0000	p_bl_p2q2 (R/W)	N	N
	P2 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13978 R0x369A	15:0	0x0000	p_bl_p2q3 (R/W)	N	N
	P2 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13980 R0x369C	15:0	0x0000	p_bl_p2q4 (R/W)	N	N
	P2 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R13982 R0x369E	15:0	0x0000	p_gb_p2q0 (R/W)	N	N
	P2 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13984 R0x36A0	15:0	0x0000	p_gb_p2q1 (R/W)	N	N
	P2 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13986 R0x36A2	15:0	0x0000	p_gb_p2q2 (R/W)		
	P2 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13988 R0x36A4	15:0	0x0000	p_gb_p2q3 (R/W)		
	P2 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R13990 R0x36A6	15:0	0x0000	p_gb_p2q4 (R/W)		
	P2 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14016 R0x36C0	15:0	0x0000	p_gr_p3q0 (R/W)		
	P3 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R14018 R0x36C2	15:0	0x0000	p_gr_p3q1 (R/W)		
	P3 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R14020 R0x36C4	15:0	0x0000	p_gr_p3q2 (R/W)		
	P3 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				

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R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14022 R0x36C6	15:0	0x0000	p_gr_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R14024 R0x36C8	15:0	0x0000	p_gr_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R14026 R0x36CA	15:0	0x0000	p_rd_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14028 R0x36CC	15:0	0x0000	p_rd_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14030 R0x36CE	15:0	0x0000	p_rd_p3q2 (R/W)		
	P3 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14032 R0x36D0	15:0	0x0000	p_rd_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14034 R0x36D2	15:0	0x0000	p_rd_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14036 R0x36D4	15:0	0x0000	p_bl_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R14038 R0x36D6	15:0	0x0000	p_bl_p3q1 (R/W)	N	N
	P3 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R14040 R0x36D8	15:0	0x0000	p_bl_p3q2 (R/W)		
	P3 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R14042 R0x36DA	15:0	0x0000	p_bl_p3q3 (R/W)		
	P3 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R14044 R0x36DC	15:0	0x0000	p_bl_p3q4 (R/W)		
	P3 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R14046 R0x36DE	15:0	0x0000	p_gb_p3q0 (R/W)	N	N
	P3 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14048 R0x36E0	15:0	0x0000	p_gb_p3q1 (R/W)		
	P3 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				

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Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14050 R0x36E2	15:0	0x0000	p_gb_p3q2 (R/W)		
	P3 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14052 R0x36E4	15:0	0x0000	p_gb_p3q3 (R/W)	N	N
	P3 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14054 R0x36E6	15:0	0x0000	p_gb_p3q4 (R/W)	N	N
	P3 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14080 R0x3700	15:0	0x0000	p_gr_p4q0 (R/W)	N	N
	P4 coefficient for Q0 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R14082 R0x3702	15:0	0x0000	p_gr_p4q1 (R/W)	N	N
	P4 coefficient for Q1 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R14084 R0x3704	15:0	0x0000	p_gr_p4q2 (R/W)		
	P4 coefficient for Q2 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R14086 R0x3706	15:0	0x0000	p_gr_p4q3 (R/W)	N	N
	P4 coefficient for Q3 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R14088 R0x3708	15:0	0x0000	p_gr_p4q4 (R/W)	N	N
	P4 coefficient for Q4 for Gr. P_GR_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gr pixels.				
R14090 R0x370A	15:0	0x0000	p_rd_p4q0 (R/W)	N	N
	P4 coefficient for Q0 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14092 R0x370C	15:0	0x0000	p_rd_p4q1 (R/W)	N	N
	P4 coefficient for Q1 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14094 R0x370E	15:0	0x0000	p_rd_p4q2 (R/W)	N	N
	P4 coefficient for Q2 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14096 R0x3710	15:0	0x0000	p_rd_p4q3 (R/W)		
	P4 coefficient for Q3 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14098 R0x3712	15:0	0x0000	p_rd_p4q4 (R/W)	N	N
	P4 coefficient for Q4 for Rd. P_RD_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Rd pixels.				
R14100 R0x3714	15:0	0x0000	p_bl_p4q0 (R/W)	N	N
	P4 coefficient for Q0 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				

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R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14102 R0x3716	15:0	0x0000	p_bl_p4q1 (R/W)		
	P4 coefficient for Q1 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R14104 R0x3718	15:0	0x0000	p_bl_p4q2 (R/W)	N	N
	P4 coefficient for Q2 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R14106 R0x371A	15:0	0x0000	p_bl_p4q3 (R/W)	N	N
	P4 coefficient for Q3 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R14108 R0x371C	15:0	0x0000	p_bl_p4q4 (R/W)	N	N
	P4 coefficient for Q4 for Bl. P_BL_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Bl pixels.				
R14110 R0x371E	15:0	0x0000	p_gb_p4q0 (R/W)	N	N
	P4 coefficient for Q0 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14112 R0x3720	15:0	0x0000	p_gb_p4q1 (R/W)	N	N
	P4 coefficient for Q1 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14114 R0x3722	15:0	0x0000	p_gb_p4q2 (R/W)	N	N
	P4 coefficient for Q2 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14116 R0x3724	15:0	0x0000	p_gb_p4q3 (R/W)	N	N
	P4 coefficient for Q3 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14118 R0x3726	15:0	0x0000	p_gb_p4q4 (R/W)	N	N
	P4 coefficient for Q4 for Gb. P_GB_PpQq registers are read successively when the row polynomial (Q) coefficients are calculated during the horizontal blanking period before a row containing Gb pixels.				
R14208 R0x3780	15:0	0x0000	poly_sc_enable (R/W)	N	N
	15	0x0000	enable 0: Lens Shading Disabled. 1: Lens Shading Enabled.	N	N
	14:0	X	Reserved		
	The POLY_SC_EN bit in this register controls the lens shading correction function.				
R14210 R0x3782	15:0	0x02A0	poly_origin_c (R/W)	N	N
	Origin of polynomial function: applied as offset to X (col) coordinate of pixel.				
R14212 R0x3784	15:0	0x01A8	poly_origin_r (R/W)		
	Origin of polynomial function: applied as offset to Y (row) coordinate of pixel.				
R14272 R0x37C0	15:0	0x0000	p_gr_q5 (R/W)	N	N
	Parameter for parabolic roll-off algorithm for greenR pixels.				
R14274 R0x37C2	15:0	0x0000	p_rd_q5 (R/W)		
	Parameter for parabolic roll-off algorithm for red pixels.				
R14276 R0x37C4	15:0	0x0000	p_bl_q5 (R/W)		
	Parameter for parabolic roll-off algorithm for blue pixels.				

Table 2: Manufacturer Specific Register Descriptions
R/W (Read or Write) bit; RO (Read Only) bit

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R14278 R0x37C6	15:0	0x0000	p_gb_q5 (R/W)		
	Parameter for parabolic roll-off algorithm for greenB pixels.				

Revision History

Rev. 1, Preview **3/4/14**

- Initial release

Rev. A **4/14/14**

- Updated to Production

Rev. 3 . . . . . **8/4/15**

- Converted to ON Semiconductor template
- Updated Table of Contents and Revision History formats
- Removed Confidential marking