Recommendations for Printed Circuit Board Assembly of Infineon SON Packages

Additional Information

DS4 2012-05

Edition 2012-05

Published by
Infineon Technologies AG
81726 Munich, Germany

© 2012 Infineon Technologies AG
All Rights Reserved.

LEGAL DISCLAIMER

THE INFORMATION GIVEN IN THIS APPLICATION NOTE IS GIVEN AS A HINT FOR THE IMPLEMENTATION OF THE INFINEON TECHNOLOGIES COMPONENT ONLY AND SHALL NOT BE REGARDED AS ANY DESCRIPTION OR WARRANTY OF A CERTAIN FUNCTIONALITY, CONDITION OR QUALITY OF THE INFINEON TECHNOLOGIES COMPONENT. THE RECIPIENT OF THIS APPLICATION NOTE MUST VERIFY ANY FUNCTION DESCRIBED HEREIN IN THE REAL APPLICATION. INFINEON TECHNOLOGIES HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND (INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY) WITH RESPECT TO ANY AND ALL INFORMATION GIVEN IN THIS APPLICATION NOTE.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Table of Contents

1 Package Description

This application note deals with Small Outline Non-leaded (SON) packages, which include various package families:

- PG-T(S)DSON packages
- PG-U(I)SON packages
- PG-V(I)SON packages
- PG-W(I)SON packages
- PG-X(I)SON packages

PG = Plastic Green
T = Thin
D = Dual
V = Very thin
W = Very, very thin
U = Ultra thin
X = Extremely thin
I = Integrated
SON = Small Outline Non-leaded

Each of these SON packages is a near-chip-scale plastic encapsulated package with a copper leadframe using perimeter lands on the bottom of the package to provide electrical and thermal contact to the Printed Circuit Board (PCB).

Representatives of the package families are:

- PG-TDSON-8: Also called SuperSO8 or S2O8, this is a leadless package that can be used on the same footprint as the DSO-8. Space in DSO packages that is occupied by the lead bending can serve as a die pad for a larger die. An important difference between the S2O8 and the DSO-8 is the extended drain connection area (exposed pad) of the PG-TDSON-8, which can offer a direct low-resistance thermal path to the board where the device is mounted if an appropriate board pad layout is used.
- PG-TDSON-8-4: The so-called Dual SuperSO8 or Dual S2O8 has the same outline as all other PG-TDSON-8 devices but has a split exposed pad that provides space for two separated Field-Effect Transistor FET-dies.
- PG-TSDSON-8: The so-called Shrink SuperSO8/S3O8 is a shrink version of the PG-TDSON-8.
- PG-TDSON-10: Also called the DFN10, this was introduced to meet the need for higher pin count and miniaturization.
- Lead-fused versions: These packages have connected source leads that serve as a combined external terminal and therefore provide an extended path for heat dissipation and current.
- PG-VISON and PG-WISON: power components in halfbridge configuration.
- PG-VSON-4: This is a high-voltage version of the so-called ThinPAK.
- PG-USON-10: Similar to TDSON-10, this package has smaller outer dimensions and a smaller die pad.
- PG-XSON-8: This is a very thin package with a big die pad for optimized thermal transfer from chip to board

Figure 1 shows photos of some representative packages.

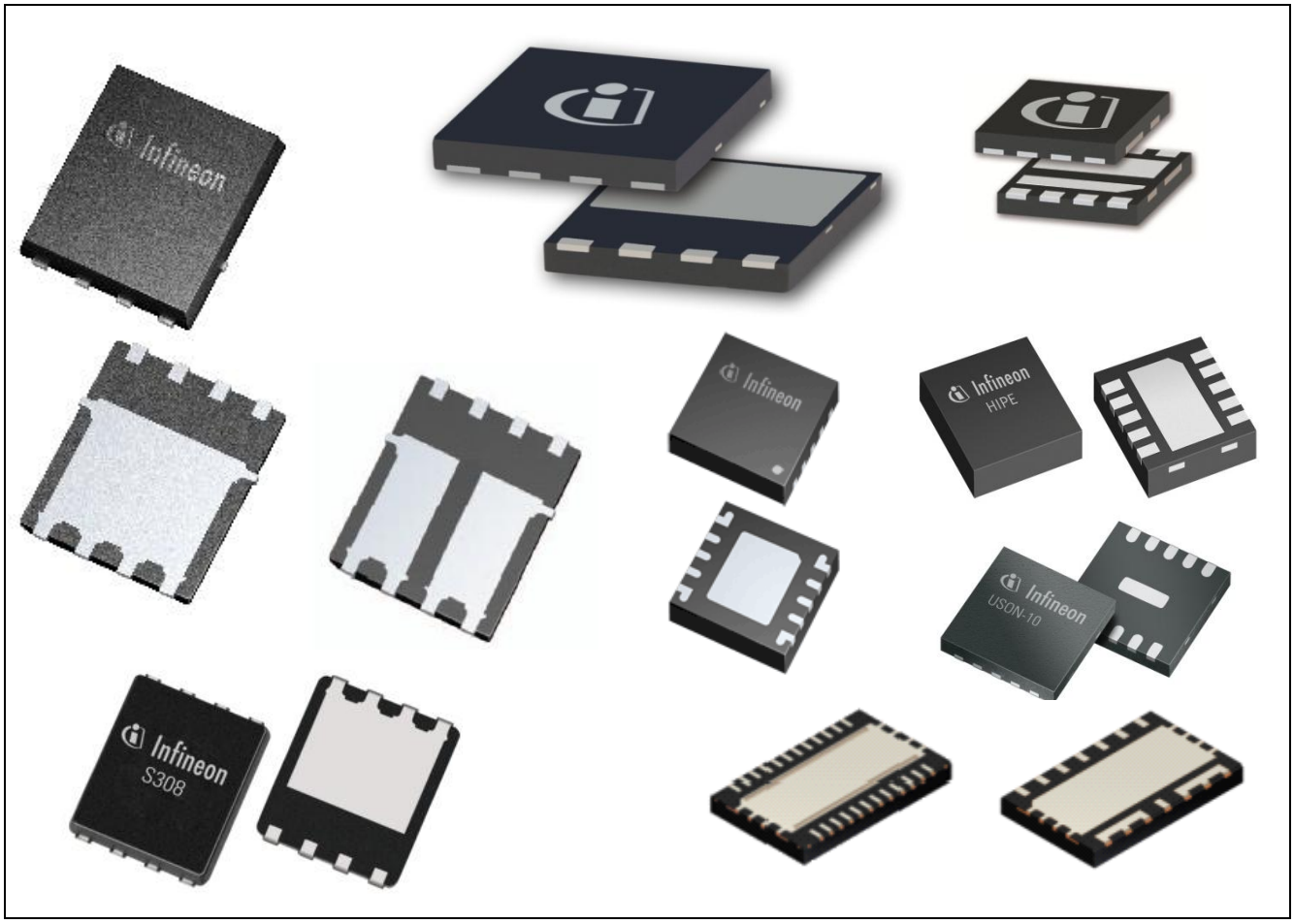

Figure 1 Single SuperSO8, Dual SuperSO8, Shrink SuperSO8, TDSON-8, WISON-8, VSON-4, USON-10, TDSON-10, VSON-10, TSON-14, TSON-24

Features

- Optimal electrical performance due to leadless land pattern
- Enhanced thermal performance through exposed die pad (drain contact) lands and exposed die pad
- Tin-plated contacts that are compatible with Pb-containing and Pb-free soldering
- Thin package
- Optimal package-to-chip ratio
- Super-SO8: Package outline complies with JEDEC MO-240
- Clip versions: Low package resistance due to copper clip interconnect technology (source contact)
- Fused lead versions: Enhanced thermal performance due to additional heat transfer through fused source area, which also prevents current crowding
- Lead Tip Inspection (LTI) feature available for specific package outlines; please contact your sales representative for more details

The die of a TDSON package can be connected electrically in various ways to the leadframe. Figure 2, 3, and4)

Figure 5 illustrates a typical LTI feature.

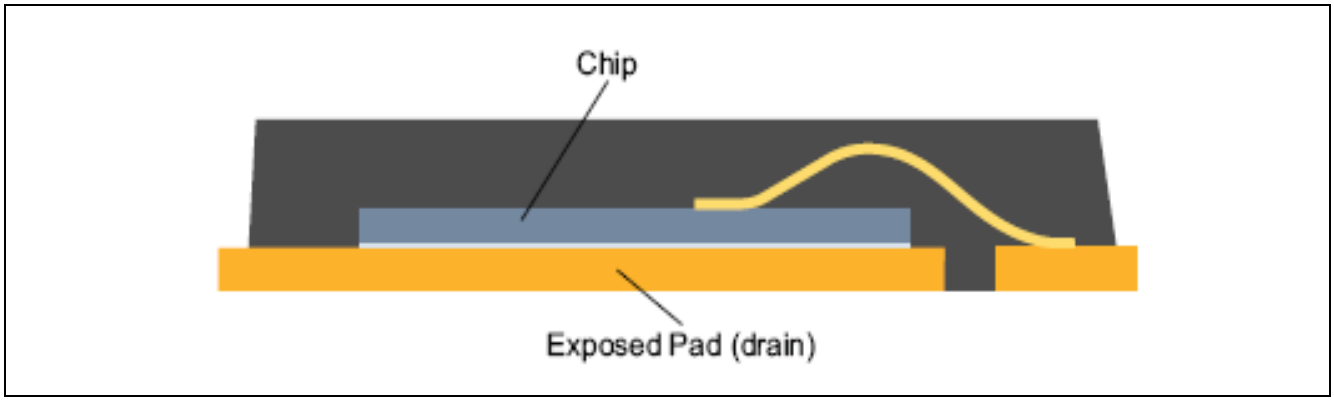

Figure 2 Cross section showing construction of a wire bond (e.g. TDSON)

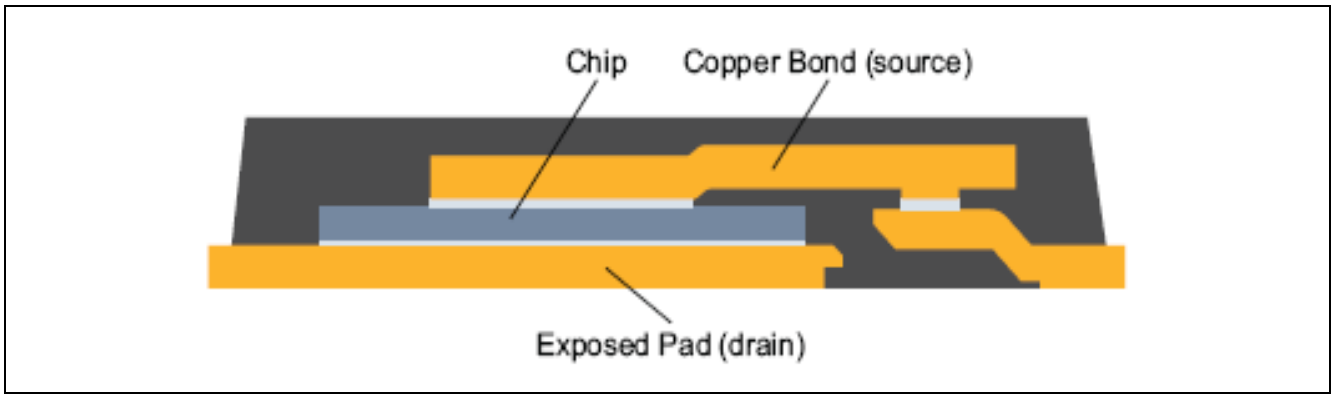

Figure 3 Cross section showing construction of a clip bond (e.g. TDSON)

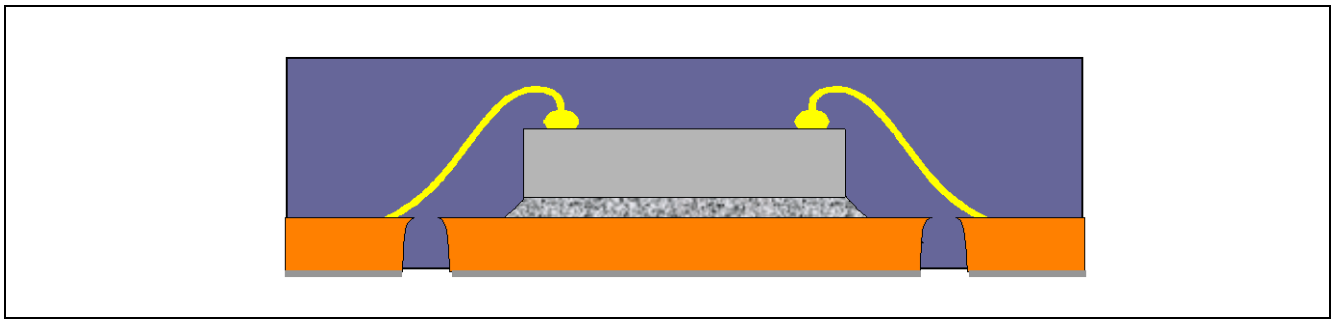

Figure 4 Cross section showing construction of a two-sided wire bond package (e.g. USON)

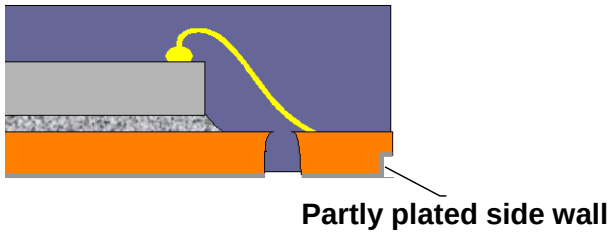

Figure 5 Schematic cross section of a LTI (lead tip inspection) feature

Semiconductor devices are sensitive to excessive electrostatic discharge, moisture, mechanical handling, and contamination. Therefore they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing. For details, please refer to the General Recommendations for Assembly of Infineon Packages in “Package Handling” (available at www.infineon.com\packages .

2 Printed Circuit Board (PCB)

2.1 Routing

PCB design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite one another on either side of a PCB if double-sided mounting is used, because that will stiffen the assembly and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, it is known that the board stiffness itself has a significant influence on the reliability (temperature cycling) of the solder joint interconnect if the system is used in critical temperature-cycling conditions.

2.2 PCB Pad Design

The interconnect solder joint-to-board is influenced by:

- General pad technology (Solder Mask Defined; short: SMD and Non Solder Mask Defined; short NSMD)
- Specific pad dimensions
- Pad finish (also called metallisation or final plating)
- Via layout and technology

Further information can be found in the General Recommendations for Assembly of Infineon Packages by following the links to “Printed Circuit Board” at www.infineon.com\packages.

The following material provides some special recommendations for Infineon SON packages containing power devices such as power Metal Oxide Semiconductor Field Effect Transistors MOSFETs.

Such power-SON packages have metallic drain-pads on the bottom side, which conduct a large amount of heat into the PCB to achieve higher thermal performance; therefore their complete area should be soldered to the PCB. The drain pad can be soldered 1:1 by area or by rectangular so-called “pockets” that reduce solder-joint voiding. In any case, the stencil aperture size under the drain pad has to be reduced to avoid device tilting.

In high-current applications or those having high thermal dissipation, source pads also require the largest possible contact area to the PCB. SMD pads are the preferred solution.

In situations that can have high currents in combination with high temperatures such as automotive applications, large conductor cross-sections are preferable to avoid electromigration. An example of a poorly designed board layout is shown in Figure 6.

Internal studies have demonstrated that Power-SON packages have good self-alignment during reflow soldering process using the following recommended layout for reflow soldering.

Further details about PCB layout recommendations can be found in Infineon’s online package data base at www.infineon.com\packages. Please choose a specific package when you are searching the data base, which includes package and packing drawings, and further package-specific information such as recommendations for PCB layout.

Please note that the recommendations can only give dimensions for the solder mask openings (if SMD is recommended) or the copper (if NSMD is recommended). Generally the smallest dimensions possible for copper pads or solder mask openings will depend on the board manufacturer. For high-current applications, SMD pads are recommended, and the copper dimensions for drain and source pads should be as big as possible to enlarge the conductor cross-sections.

Please note that there is no exact congruency of PCB pads and package pads.

For suitable wave soldering layouts for Power-SON packages, please refer to Section 4.2.

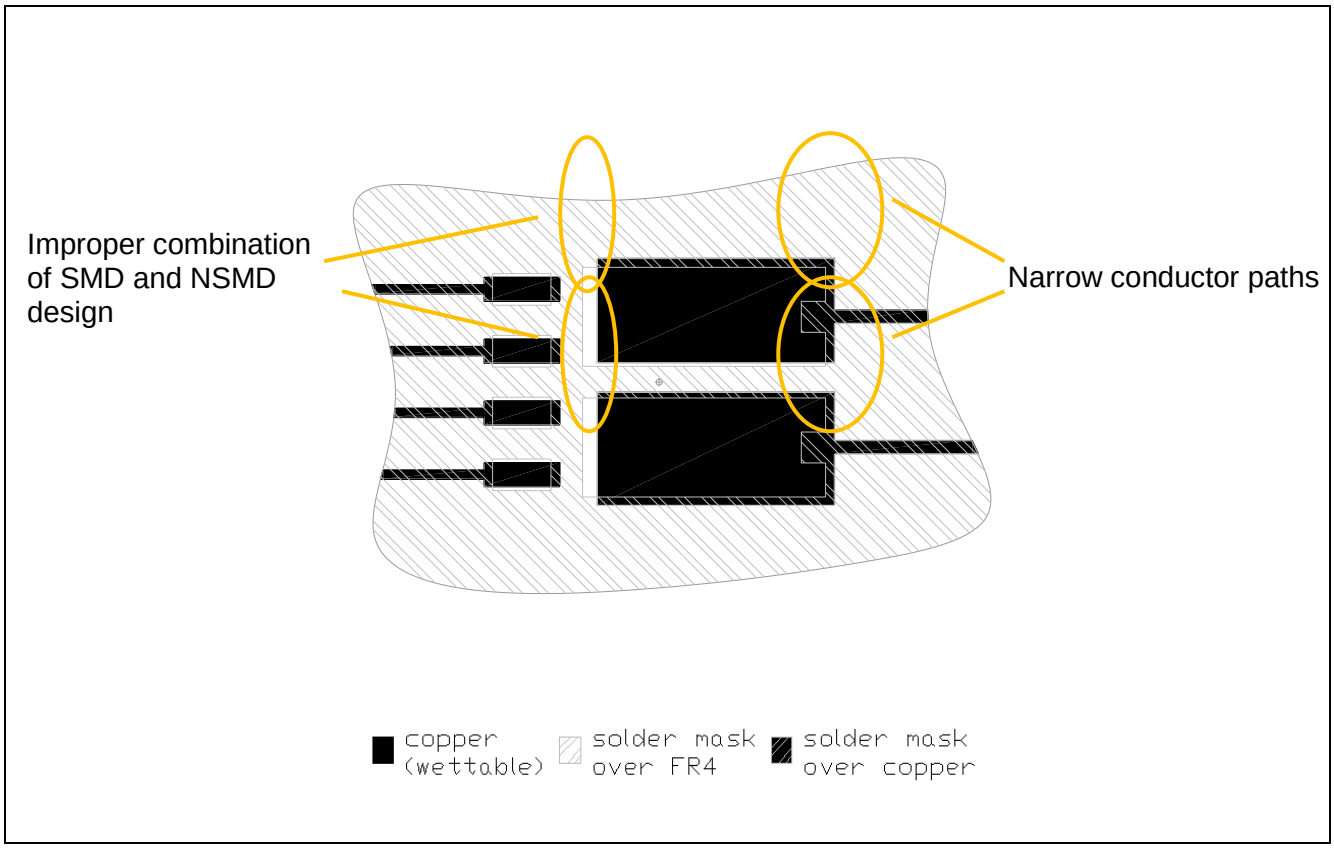

Figure 6 Example of poor PCB layout. Narrow conductor paths limit current and thermal flow. Mixing of SMD and NSMD lead to improper pad definition.

To connect the exposed die pad thermally and electrically directly to inner and/or bottom copper planes of the board, plated through-hole vias are used. They help to distribute the heat into the board area. The heat spreads from the chip over the package die pad and the solder joint to the thermal pad on the board.

A typical hole diameter for such thermal vias is 0.2 - 0.4 mm. The diameter and the number of vias in the thermal pad depend on the thermal requirements of the end product, the power consumption of the product, the application, and the construction of the PCB. However, an array of thermal vias with pitch 1.0-1.2 mm can be a reasonable starting point for further optimization of most products/applications. Thermal and electrical analysis and/or testing are recommended to determine the minimum number of vias needed.

A good solder joint at the central die pad can be formed using vias that remain open on both sides of the board. However, there are two things to be considered. Open vias in the thermal pad will lead to a lower stand off between package and board. This is mostly controlled by the solder volume between the package die pad and thermal pad on the PCB. In addition, solder can protrude to the other side of the board, which may interfere with a second solder paste printing process on this opposite board side. To prevent solder beading, a wettable surface surrounding these vias on the opposite board side should be provided to act as a buffer for the surplus solder. It is also recommended to arrange the vias symmetrically in the thermal pad.

If necessary vias can be closed by “tenting”, which means the vias are covered with soder mask (e.g. dry-film solder mask). If the via tenting is done only on the opposite side of the board, the voiding rate

will increase significantly. Combined with an intelligent solder mask layout for the thermal pad (segmentation of the thermal pad using solder mask bars), this method leads to good processability and balanced solder joints.

Another method to close vias is called “plugging” (filling with epoxy), followed by overplating. Very small vias (100 µm in diameter or smaller) should be filled with copper and overplated. In both cases the specification of a planar filling is necessary to avoid cavities which will work as traps for gases, forming voids during reflow soldering.

If it is not necessary to have a direct connection from the solder pad under the exposed die pad to the inner layers of the PCB, the vias should be placed next to the footprint near the package and covered with solder mask.

Besides the power-SON packages described above, there are also Infineon SON packages containing devices that require lower thermal package performance, e.g. USON-x. When it comes to PCB design, those packages should be handled like VQFN packages. Although a fillet formation at the side wall of the leads is not guaranteed (there is no plating at the side wall of the leads), we advise you to design an extended pad at the perimeter lands to allow a solder joint fillet to develop at the side wall of the lead. Other influencing factors for fillet formation are package exposure to environment, solder paste material, and the reflow process.

If an SON package with the LTI feature is used, a solder joint fillet at the side wall of the SON land is enabled, because an LTI feature provides a partly plated and therefore wettable side wall at the lead. If fillets are formed, they will improve the reliability of the solder joint.

If the central die pad is not used as a “thermal pad” (as described above), it is a connection to ground. Using a PCB pad of the same size as the package pad will increase the solder joint reliability, and the electrical performance for some applications.

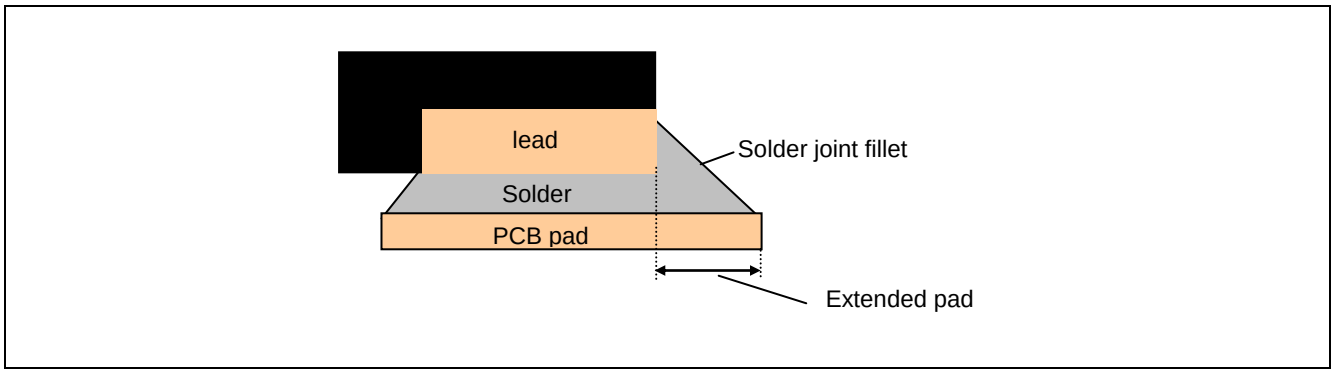

Figure 7 Schematic cross section of a perimeter lead

3 PCB Assembly Using Solder Paste Printing and Reflow Soldering

Surface Mount Devices (SMDs) are typically used in so-called Surface Mount Technology (SMT). SMT processes include solder-paste printing, pick & place, and reflow soldering.

Internal investigations have shown that some of the Power-SON packages can be wave soldered, a technique that is typically used in Through Hole Technology (THT).

This chapter discusses SMT. For information about wave soldering, please refer to Chapter 4.

3.1 Solder Stencil

The solder paste is applied onto the PCB metal pads by stencil printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. Too much solder paste will cause solder bridging, whereas too little solder paste can lead to insufficient solder wetting between all contact surfaces. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB. For typical Power-SON packages, 120- to 150-µm thick stencils are recommended (for small pitch versions, a 100-µm thick stencil is recommended).

To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut stencils (mostly made from stainless steel) are preferred.

The apertures in general should be of the same size and shape as the metal pads on the PCB. However, during the solder print operation, the squeegee bends down into larger openings so that less solder is deposited. To reduce this effect, the stencil opening for the exposed drain pad can be segmented into smaller areas (“pockets”). This reduction of solder also prevents device tilting and higher voiding rates. Infineon’s internal investigations showed that the ratio between stencil openings and drain pad can vary between 40% and 80%. The ideal amount of solder depends on stencil thickness, PCB pad finish, via layout, and solder pastes.

Further details and specific stencil aperture recommendations can be found in Infineon’s package data base at www.infineon.com\packages. Please choose a specific package when you are searching the data base, which will then show you an example of the stencil aperture layout for each package.

Please note that the recommendations are only rough guidelines. The ideal layout for a specific application depends on the factors mentioned in this document. For instance, typical boundary conditions in IFX internal investigations are no vias in the pad and 120-µm stencil thickness.

3.2 Solder Paste

Solder paste consists of solder alloy and a flux system. Normally the volume is about 50% alloy and 50% flux and solvents. In term of mass, this means approximately 90 wt% alloy and 10 wt% flux and solvents. The flux system has to remove oxides and contamination from the solder joints during the soldering process. The capacity for removing oxides and contamination is given by the relative activation level.

The contained solvent adjusts the viscosity needed for the solder paste application process. The solvent has to evaporate during reflow soldering.

Pb-free solder pastes typically contain SAC305 (3.0 % Ag and 0.5 % Cu) or other so-called SnAgCu (SAC) alloys (typically 1-4% Ag and <1% Cu).

A “no-clean” solder paste is preferred for packages such as Power-SONs where cleaning below the component is difficult.

The paste must be suitable for printing the solder stencil aperture dimensions; the usage of paste type 3 or a higher type is recommended.

Solder paste is sensitive to age, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.3 Component Placement

Although the self-alignment effect due to the surface tension of the liquid solder will support the formation of reliable solder joints, the components have to be placed accurately depending on their geometry. Positioning the packages manually is not recommended but is possible, especially for packages with big terminals and pitch. An automatic pick-and-place machine is recommended to get reliable solder joints.

Component placement accuracies of +/-50 µm are obtained with modern automatic component placement machines using vision systems. With these systems, both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). These fiducials are detected by a vision system immediately before the mounting process.

Recognition of the packages is performed by a special vision system, enabling the complete package to be centered correctly.

The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB. For example, for Shrink SuperSO8 packages with 0.3-mm pad width, the device-pad-to-PCB-pad misalignment has to be less than 60 µm to assure a robust mounting process (even if the self-centering effect during reflow soldering may allow much more misplacement). Generally this is achievable with a wide range of placement systems.

For SuperSO8 and Dual SuperSO8 packages for example, the smallest width is 0.65 mm and therefore misplacement can be up to 130 µm.

For details about factors influencing the component placement please refer to the General Recommendations for Assembly of Infineon Packages in “Mounting of SMDs” (available at www.infineon.com\packages).

3.4 Reflow Soldering

Soldering determines the yield and quality of assembly fabrication to a very large extent. Generally all standard reflow soldering processes are of one of the following types:

- Forced convection (max. qualified profile given by the JEDEC MSL classification)
- Vapor phase
- Infrared (with restrictions)

Typical temperature profiles in these methods are suitable for board assembly of the Power-SON packages.

During the reflow process, each solder joint has to be exposed to temperatures above the solder melting point or “liquidus” for a sufficient time to get the optimum solder joint quality, whereas overheating the PCB with its components has to be avoided.

Power-SON packages are qualified according to IPC/JEDEC J-STD-020. Please refer to the bar code label on the packing for the maximum peak package body temperature.

When using infrared ovens without convection, special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with components that have different thermal masses. The recommended type of process is forced-convection reflow.

Using a nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary for soldering tin-lead metal alloys.

Figure 7 shows a general forced-convection reflow profile suitable for soldering Power-SON packages.

Table 1 is an example of the key data of such a reflow profile that can be used for the Pb-free alloys listed above.

For further details about the reflow profile (especially for Pb-containing solder pastes), please refer to the General Recommendations for Assembly of Infineon Packages in “Mounting of SMDs,” available at www.infineon.com\packages).

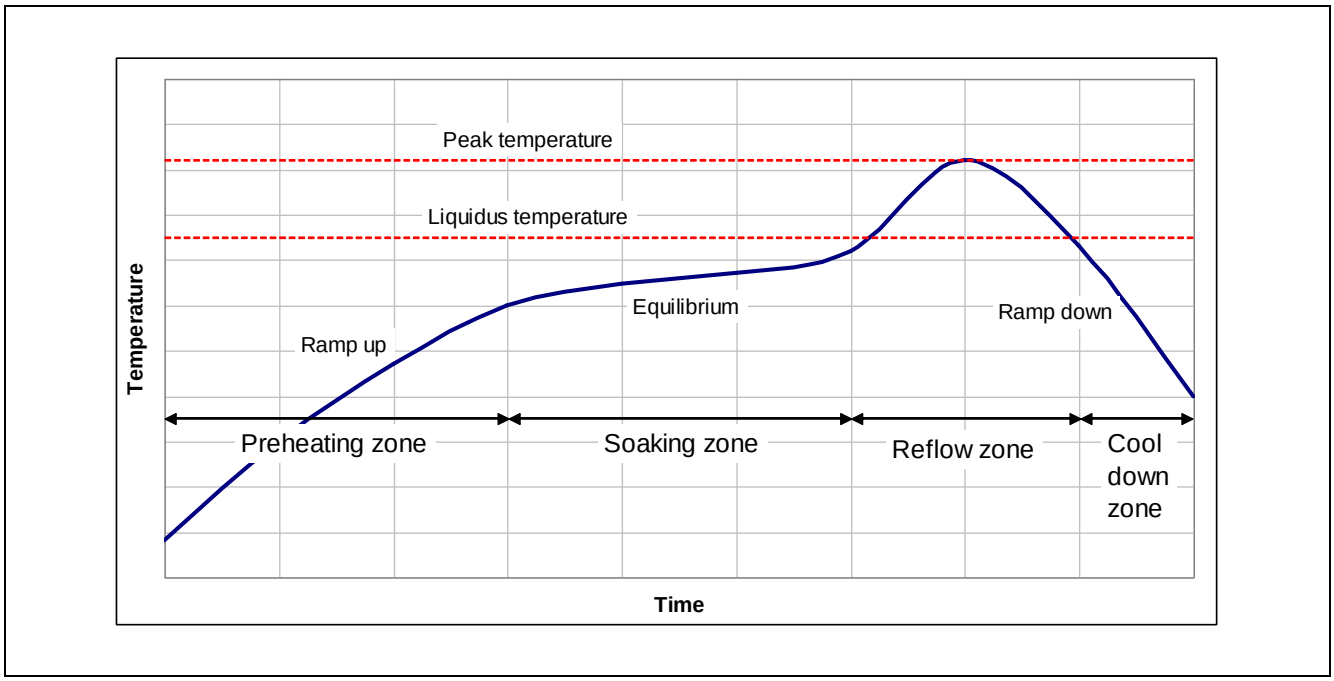

Figure 8 General forced-convection reflow solder profile

Table 1 EXAMPLE of the key data for a forced-convection reflow solder profile

parameter	minimum value	typical value	max. value (acc. IPC/ JEDEC J-STD-020)	main influence
preheating rate	1.0 K/s	2.5 K/s	3.0 K/s	flux system (solder paste)
soaking temperature	140 – 170°C	140 – 170°C	150 – 200°C	flux system (solder paste)
soaking time	50 s	80 s	120 s	flux system (solder paste)
peak temperature	230°C	245°C	260°C	alloy (solder paste)
reflow time above melting point (liquidus)	40 s	60 s	150 s	alloy (solder paste)
cool-down rate	1.0 K/s	2.5 K/s	8.0 K/s	

Double-Sided Assembly

SON packages are generally suitable for mounting on double-sided PCBs. First, the board assembly is done on one side of the PCB (including soldering). Afterwards, the second side of the PCB is assembled.

If the solder-joint thickness is a critical dimension, please be aware that solder joints of components on the first side will be reflowed again in the second reflow step. In the reflow zone of the oven (i.e. where the solder is liquid), the components are only held by wetting forces from the molten solder. Gravity acting in the opposite direction will elongate the solder joints, unlike joints on the top side, where gravity forces the components nearer to the PCB surface. This shape will be frozen at temperatures below the melting point of solder and therefore result in a higher stand-off on the bottom side after the reflow process. Heavy vibrations in a reflow oven may cause devices to drop off the PCB.

4 Wave Soldering

A product's suitability for wave soldering depends on two factors. First is its ability to withstand the heat shock. On the other hand, its processability, e.g. proper board layout and glue application, have to be taken into account.

Wave soldering of some Power-SON packages is possible, but the position of the SMD glue has to be chosen carefully. Internal investigations have proven that a proper pad layout and glue dispensing pattern can be found to have good processability prior and during wave soldering.

To determine the suitability of a given product for wave soldering, please refer to the product data sheet or ask your local IFX sales, marketing, or application engineer.

The heat shock resistance of any specific product in an SON package is determined according to JEDEC JESD22A11A.

4.1 Process Flow for SMD Devices in a Wave Soldering Process

Before SMD packages can be wave soldered, they have to be attached to the PCB by glue. The sequence for this is shown in Figure 9. These are the steps:

1. Setting of glue dots
2. Placement of SMDs
3. Curing of adhesive
4. Turning PCB
5. Wave soldering of SMDs

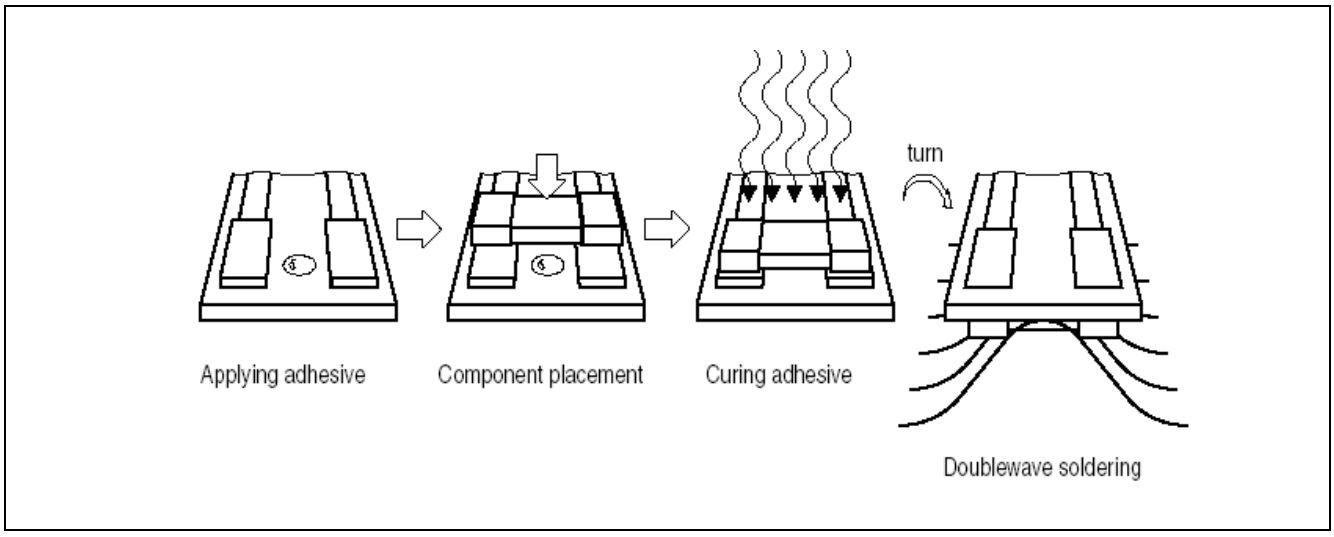

Figure 9 Attachment of SMD devices prior to wave soldering

4.2 PCB Design and SMD Glue-Dot Application for Wave Soldering

Special PCB designs and SMD glue-dot patterns are needed to give good soldering results in terms of wetting behavior, voiding rate, and co-planarity of the device.

Specific PCB pad designs for wave soldering can be found in Infineon's package data base at www.infineon.com\packages. Please choose a specific package when searching in order to find package and packing drawings, and further package-specific information such as the details about PCB layout.

For some packages, both 2-dot and 4-dot layouts for SMD glue application are feasible. The latter provides four areas for application of SMD glue. Internal investigations have proven that both versions work very well if the dots are half underneath the package and half protruding. Nevertheless the 4-dot layout has some advantages, because it prevents device tilting, which in the worst case may prevent the solder from wetting the drain pad completely. On the other hand, dispensing glue for the 2-dot layout is faster, and must be used for small packages that have less space for glue dots.

The glue should not spread over the wettable surface of pads. Even if the surface seems to be free of glue, "bleeding" can contaminate the surface and may lead to non-wetting.

After dispensing SMD glue, the component has to be assembled onto the PCB (please refer to Section 3.3). During touchdown, placement force has to be controlled in order to prevent the glue from squeezing out.

Subsequently the SMD glue has to be cured. Typically THDs are assembled afterwards and the PCB is ready for wave soldering.

Please note that the given board pad layouts are suitable and tested for a transport direction for example as shown in Figure 10.

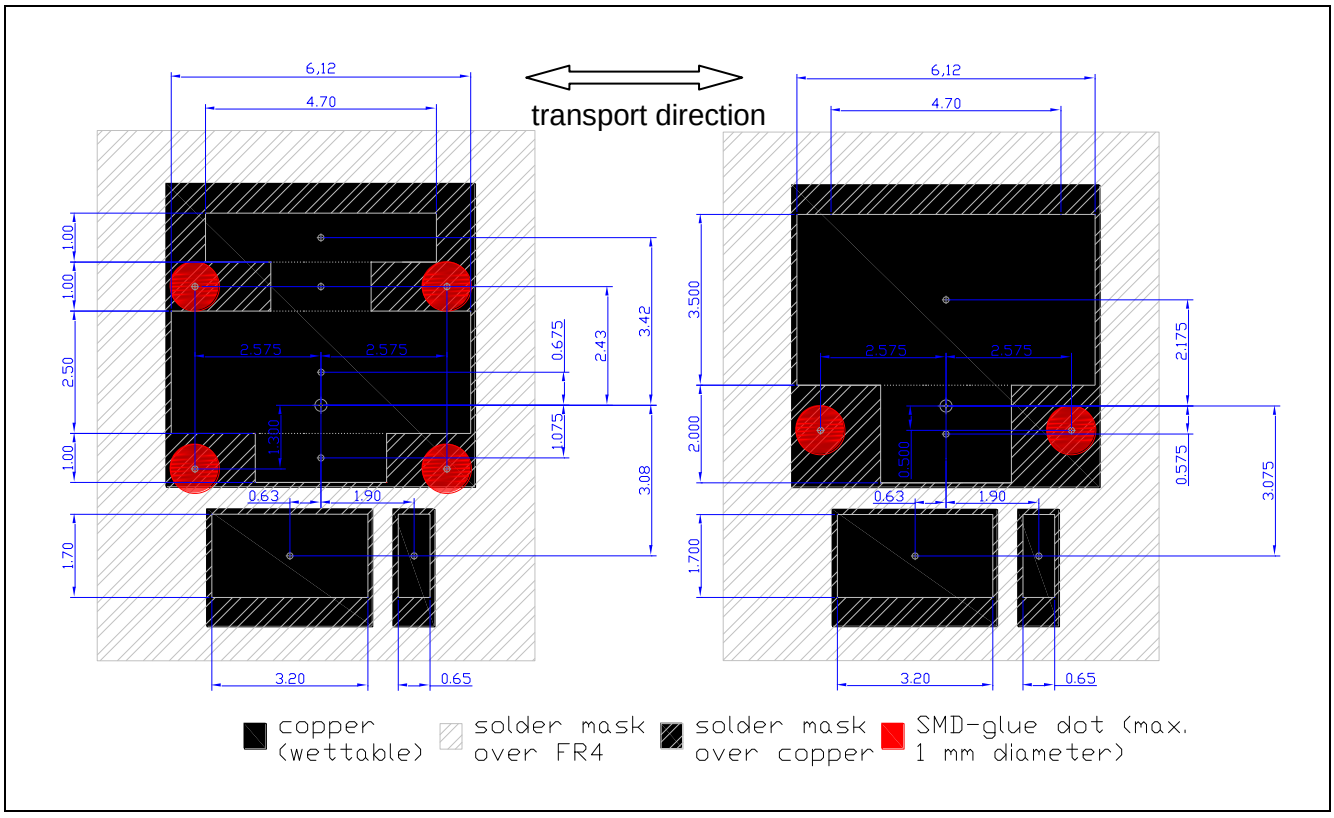

Figure 10 PCB pad designs for wave soldering of SuperSO8; left side: 4-dot version; right side: 2-dot version

4.3 Wave-soldering Temperature Profile

There are many types of wave-soldering machines. However, the basic components and principles of these machines are the same. A standard wave-solder machine has three or four zones: the fluxing zone, the preheating zone, and the soldering zone. An additional fourth zone is used for the cleaning of the board, depending on the flux type used.

Dual-wave soldering is the most common method. Figure 11 shows a typical temperature profile. The peak temperatures, ramp rates, and times depend on the materials, wave soldering equipment, and process parameters used. It is important to keep peak temperature below 260°C and the time at this temperature below 10 seconds to avoid any component damage and a reliability reduction.

The first wave has a turbulent flow and therefore guarantees wetting of nearly all shapes of leads and board pads, but also creates some solder bridges. These solder bridges have to be removed by the second wave, which has a laminar flow.

Another wave type is the so-called Wörthmann wave, which combines turbulent and laminar flow in one and therefore results in only one temperature peak.

When using Pb-free solder alloys, a nitrogen atmosphere is recommended.

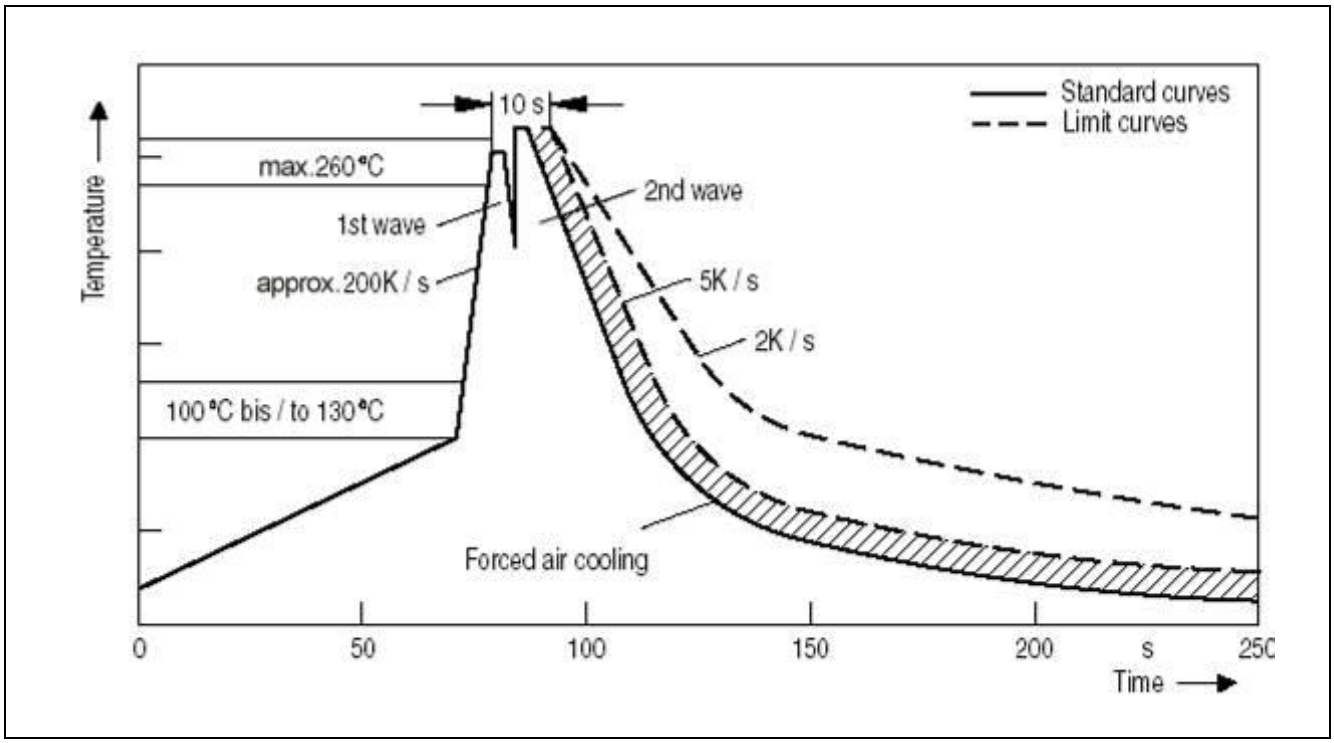

Figure 11 Typical temperature profile of a dual-wave soldering process

5 Cleaning

After the reflow or wave soldering process, some flux residues can be found around the solder joints or spreading over the whole PCB. If a “no-clean” solder paste has been used for solder paste printing (or a no-clean flux in case of wave soldering), the flux residues usually do not have to be removed after the soldering process. Cleaning beneath a Power-SON package is difficult because of the small gap between package substrate and PCB, and is therefore not recommended. If the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray, or vapor cleaning) and solution have to be selected while taking into account the kinds of packages to be cleaned, the flux used in the solder paste (rosin-based, water-soluble, etc.), and environmental and safety aspects. Even small residues of the cleaning solution should be removed/dried very thoroughly. Contact the solder paste or flux manufacturer for recommended cleaning solutions.

6 Inspection

Compared to typical SMD components that have gullwing leads, for example, the solder joints of Power-SON packages are mainly formed underneath the package. The leads end directly at the component body edge barely protrude. A visual inspection of the solder joints with conventional Automatic Optical Inspection (AOI) systems is limited to the outer surface of the solder joints. Since the non-wetting of the package lead front-side walls is not a rejection criterion, the usefulness of an optical inspection is questionable. If a package is equipped with an LTI feature, wetting of the lead side wall is possible because an LTI feature provides a partly plated lead side wall. Figure 12 shows solder joints of a SuperSO8, which are comparable of those of Dual SuperSO8. For the Shrink SuperSO8, the visibility is limited because the leads do not protrude beyond the package body.

For the acceptability of electronic assemblies inspected optically, please refer also to the IPC-A-610 standard.

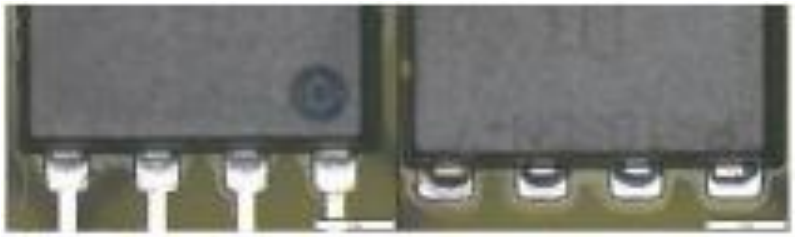

Figure 12 Typical optical photos of SuperSO8 solder joints. Those of gate and source can be seen on the left side. The right side shows the four soldered extensions of the big drain pad.

Automatic X-ray Inspection (AXI) systems are appropriate for efficient inline control. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing, and data transfer routines. These reliable systems enable the user to detect soldering defects such as poor soldering, bridging, voiding, and missing parts. However, other defects such as broken solder joints are not easily detectable by X-ray.

Figure 13 shows some typical X-ray photos of SuperSO8 and Shrink SuperSO8 packages. Internal solder joints, wire- and clipbonds, leadframe, and the solder joints that connect the package to the PCB are all visible. The big drain pad voids formed during soldering can easily be seen. The solder pads used are SMD and have no vias in the pad.

As a rule-of-thumb, a 25% maximum voiding rate (X-ray inspection top-down view) for the perimeter pads is a starting point. The bigger exposed pad may tend to more or less voiding, depending on board pad size, via and stencil layout, solder paste, and reflow profile. Generally such big solder pads do not provide enough surface for gas that is generated during reflow to escape. Therefore, solder joints of big pads generally tend to show more voiding.

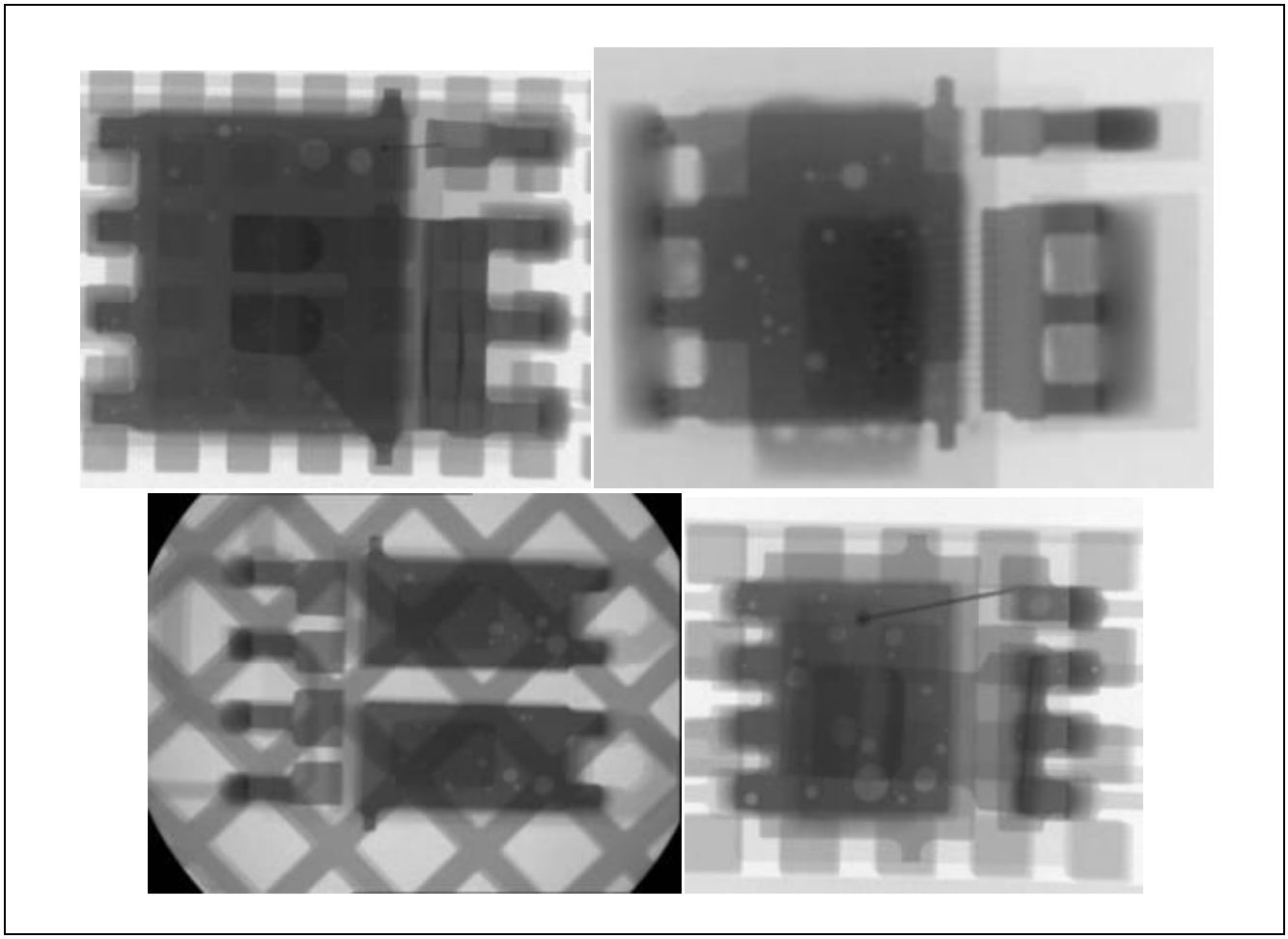

Figure 13 X-ray photos of a reflow-soldered SuperSO8 (top left), a wave-soldered SuperSO8 (top right), a reflow-soldered Dual SuperSO8 (center), and a reflow-soldered Shrink SuperSO8 (bottom)

Cross-sectioning of a soldered package as well as dye penetrant analysis can serve as tools for sample monitoring only, because of their destructive character. Nonetheless, these analysis methods must be used during engineering of new products at customers' production sites to get detailed information about the solder-joint quality. Figure 14 shows typical cross-sections through solder joints. The first photo shows the outer part of the solder joint of the big drain pad with a partly formed meniscus (wetting not necessary according to IPC-A-610). The second photo shows the outer part of the solder joint of a gate pad (same for source pad) that shows a well-formed meniscus.

Pb-free solder joints look different from tin-lead (SnPb) solder joints. SnPb solder joints typically have a bright and shiny surface. Lead-free (SnAgCu) solder joints typically do not have this bright surface. Pb-free solder joints are often dull and grainy. These surface properties are caused by the irregular solidification of the solder, as the solder alloys are not exactly eutectic (like the 63Sn37Pb solder alloy). This means that SnAgCu-solders do not have a melting point but a melting range of several degrees. Although Pb-free solder joints have this dull surface, this does not mean that Pb-free joints are of lower quality or weaker than SnPb joints. It is therefore necessary to teach the inspection staff what these Pb-free joints look like, and/or to adjust optical inspection systems to handle Pb-free solder joints.

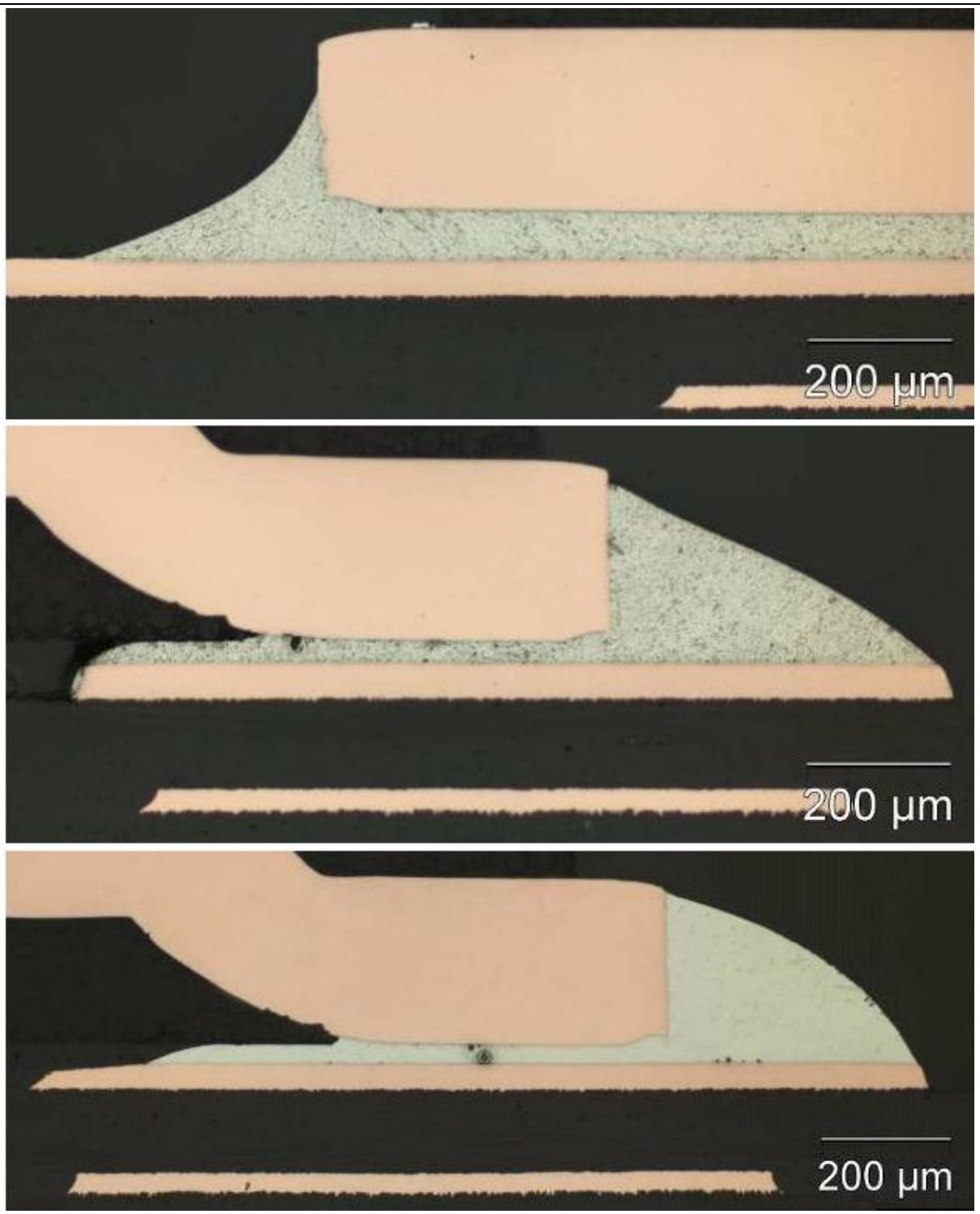

Figure 14 Cross-section views of mounted TDSON-8 packages. The first photo shows a SnPb solder joint of the drain pad. The second and third photos show source/gate solder joints with SnPb, and SnAgCu alloys, respectively.

7 Rework

If a defective component is detected after board assembly, the device can be removed and replaced by a new one. Due to possible damage while removing the component, a desoldered component should not be reused.

Desoldering the old component (if analysis afterwards is planned) and resoldering of the new component has to be done very thoroughly.

Single solder joint repair of Power-SON packages is very difficult, if not impossible, and therefore not recommended at all.

Follow these instructions prior to and during rework process:

- **Dry the PCB and components prior to rework.** A proper drying procedure for SMD packages is described in the international standard IPC/JEDEC J-STD-033. Please also refer to the recommendations of your PCB manufacturer and take all specific needs of components, PCB, and other materials into account.
- **Use tools that do not damage the component mechanically.** Please note that mechanical forces need not necessarily cause external damage, which could be detected more easily, but may cause internal damage and reduce the component's reliability. A proper handling system with vacuum nozzle may be the most gently process and is therefore recommended. However, the impact of rework tools has to be assessed properly.
- Whatever heating system is used (hot air, infrared, hot plate, etc.), ensure that the applied temperature profile at the **component never exceeds the maximum profile specified in the international standard IPC/JEDEC J-STD-020.** Internal investigations have shown that the temperature profile must be recorded.
- In general, more manual handling increases the effort for documentation, training, and monitoring of the rework process(es). Investigations have shown that if distance, time, and airflow are properly controlled, a hot air temperature of 300°C can be used, for example, without violating the maximum allowed reflow profile. On the other hand, when other process parameters were changed, the same hot air temperature setting was able to heat up the component to above 280°C, which exceeds the component's specification by far.
- If a desoldered component might be reused, please consider that components are qualified to withstand a maximum of three reflow cycles. In this specific case, two cycles have already occurred during rework, and only one is left for the board assembly.

For further information about tooling and process steps for rework, please refer to the General Recommendations for Assembly of Infineon Packages in the "Rework" section at http://www.infineon.com/packages).

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG