

Op Amp Precision Design: PCB Layout Techniques

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INTRODUCTION

This application note covers Printed Circuit Board (PCB) effects encountered in high (DC) precision op amp circuits. It provides techniques for improving the performance, giving more flexibility in solving a given design problem. It demonstrates one important factor necessary to convert a good schematic into a working precision design.

This material is for engineers who design slow precision circuits, including those with op amps. It is aimed at those engineers with little experience in this kind of design, but can also help experienced engineers that are looking for alternate solutions to a design problem.

The information in this application note can be applied to all precision (DC) analog designs, with some thought and diligence. The focus is on common op amp circuits so that the reader can quickly convert this material into improvements in their own op amp designs.

Additional material at the end of the application note includes references to the literature and the schematic of a PCB used in the design example.

Key Words and Phrases

- Op Amp
- Temperature
- Thermal Gradient
- Thermocouple Junction
- Thermoelectric Voltage
- IC Sockets
- Contact Potential
- PCB Surface Contamination

Related Application Notes

The following application notes, together with this one, form a series about precision op amp design topics. They cover both theory and practical methods to improve a design's performance.

- AN1177 on DC Errors [2]
- AN1228 on Random Noise [3]

THERMOCOUPLE JUNCTION BEHAVIOR

While thermocouples are a common temperature sensor [5], it is not commonly known that every PCB design includes many unintended thermocouple junctions that modify the signal voltages. This section covers the physics behind this effect and gives practical illustrations.

Seebeck Effect

When two dissimilar conductors (or semiconductors) are joined together, and their junction is heated, a voltage results between them (Seebeck or thermoelectric voltage); this is known as the Seebeck effect. This voltage is roughly proportional to absolute temperature. There are many references that discuss this effect in detail, including the "Temperature Products" section of reference [8]; see especially pages Z-13, Z-14 and Z-23 through Z-32.

Figure 1 shows the Seebeck voltage as a function of temperature for the standard type K thermocouple. Notice that the response is not strictly linear, but can be linearized over small temperature ranges (e.g., $\pm 10^{\circ}\text{C}$).

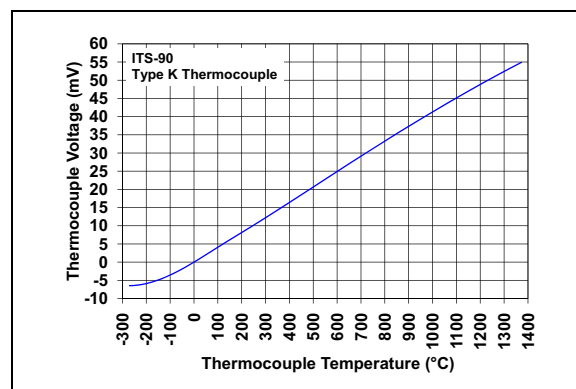


FIGURE 1: Type K Thermocouple's Response.

Most thermocouple junctions behave in a similar manner. The following are examples of thermocouple junctions on a PCB:

- Components soldered to a copper pad
- Wires mechanically attached to the PCB
- Jumpers
- Solder joints
- PCB vias

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The linearized relationship between temperature and thermoelectric voltage, for small temperature ranges, is given in Equation 1. The Seebeck coefficients for the junctions found on PCBs are typically, but not always, below $\pm 100 \mu\text{V}/^\circ\text{C}$.

EQUATION 1: SEEBECK VOLTAGE

$$\Delta V_{TH} \approx k_J(T_J - T_{REF})$$

$$V_{TH} = V_{REF} + \Delta V_{TH}$$

Where:

- ΔV_{TH} = Change in Seebeck voltage (V)
- k_J = Seebeck coefficient ($\text{V}/^\circ\text{C}$)
- T_J = Junction Temperature ($^\circ\text{C}$)
- T_{REF} = Reference Temperature ($^\circ\text{C}$)
- V_{TH} = Seebeck voltage (V)
- V_{REF} = Seebeck voltage at T_{REF} (V)

Illustrations Using a Resistor

Three different temperature profiles will be shown that illustrate how thermocouple junctions behave on PCB designs. Obviously, many other components will also produce thermoelectric voltages (e.g., PCB edge connectors).

Figure 2 shows a surface mount resistor with two metal (copper) traces on a PCB. The resistor is built with end caps for soldering to the PCB and a very thin conducting film that produces the desired resistance. Thus, there are three conductor types shown in this figure, with four junctions.

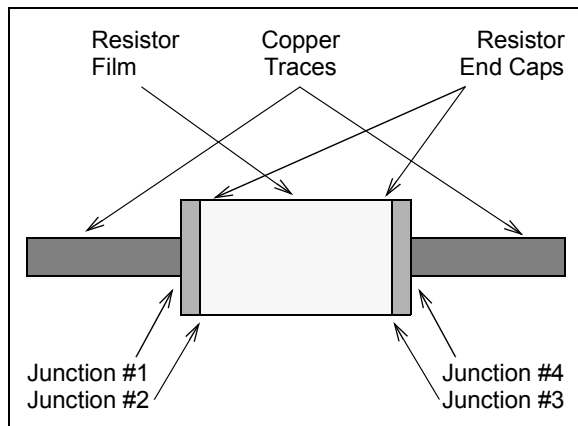


FIGURE 2: Resistor and Metal Traces on PCB.

For illustrative purposes, we'll use the arbitrary values shown in Table 1. Notice that junctions 1 and 4 are the same, but the values are shown with opposite polarities; this is one way to account for the direction current flows through these junctions (the same applies to junctions 2 and 3).

TABLE 1: ASSUMED THERMOCOUPLE JUNCTION PARAMETERS

Junction No.	V_{REF} (mV)	k_J ($\mu\text{V}/^\circ\text{C}$)
1	10	40
2	-4	-10
3	4	10
4	-10	-40

- Note 1:** V_{REF} and k_J have polarities that assume a left-to-right horizontal direction.
Note 2: $T_{REF} = 25^\circ\text{C}$.

CONSTANT TEMPERATURE

In this illustration, temperature is constant across the PCB. This means that the junctions are at the same temperature. Let's also assume that this temperature is $+125^\circ\text{C}$ and that the voltage on the left trace is 0V. The results are shown in Figure 3. Notice that V_{TH} is the voltage change from one conductor to the next.

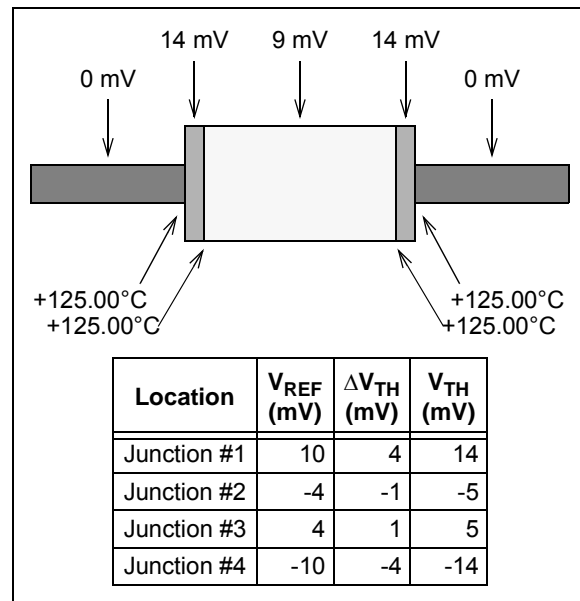


FIGURE 3: Constant Temperature Results.

TEMPERATURE CHANGE IN THE NORMAL DIRECTION

In this illustration, temperature changes vertically in Figure 2 (normal to the resistor's axial direction), but does not change in the axial direction (horizontally).

The metal areas maintain almost constant voltages in the normal direction, so this case is basically the same as the previous one.

Note: When temperature is constant along the direction of current flow, the net change in thermoelectric voltage between two conductors of the same material is zero.

TEMPERATURE CHANGE IN THE AXIAL DIRECTION

In this illustration, temperature changes horizontally in [Figure 2](#) (along the resistor's axial direction), but does not change in the normal direction (vertically). Let's assume 0V on the left copper trace, +125°C at Junction #1, a temperature gradient of 10°C/in (0.394°C/mm) from left to right (0 in the vertical direction) and a 1206 SMD resistor.

The resistor is 0.12 inches long (3.05 mm) and 0.06 inches wide (1.52 mm). Assume the end caps are about 0.01 inches long (0.25 mm) and the metal film is about 0.10 inches long (2.54 mm). The results are shown in [Figure 4](#).

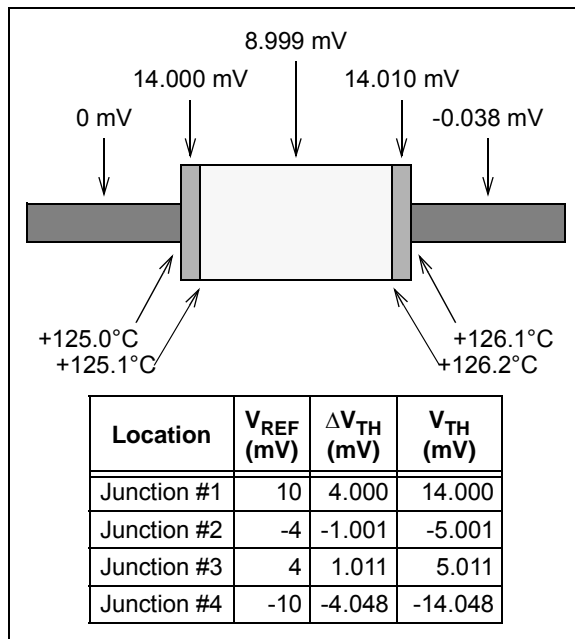


FIGURE 4: Axial Gradient Results.

Thus, the temperature gradient of 10°C/in (1.2°C increase from left to right) caused a total of -38 μV to appear across this resistor. Notice that adding the same temperature change to all junction temperatures will not change this result.

Note: Shifting all of the junction temperatures by the same amount does not change the temperature gradient. This means that the voltage drop between any two points in the circuit using the same conductive material is the same (assuming we're within the linear region of response).

PREVENTING LARGE THERMOELECTRIC VOLTAGES

This section includes several general techniques that prevent the appearance of large temperature gradients at critical components.

Reduced Heat Generation

When a PCB's thermal gradient is mainly caused by components attached to it, then find components that dissipate less power. This can be easy to do (e.g., change resistors) or hard (change a PICmicro[®] microcontroller).

Increasing the load resistance, and other resistor values, also reduces the dissipated power. Choose lower power supply voltages, where possible, to further reduce the dissipated power.

Redirect the Heat Flow

Changing the direction that heat flows on a PCB, or in its immediate environment, can significantly reduce temperature gradients. The goal is to create nearly constant temperatures in critical areas.

ALTERNATE HEAT PATHS

Adding heat sinks to parts that dissipate a lot of power will redirect the heat to the surrounding air. One form of heat sink that is often overlooked is either ground planes or power planes in the PCB; they have the advantage of making temperature gradients on a PCB lower because of their large (horizontal) thermal conductivity.

Adding a fan to a design will also redirect heat to the surrounding air, which reduces the temperature drop on the PCB. This approach, however, is usually avoided to minimize other design issues (random temperature fluctuations, acoustic noise, power, cost, etc.). It is important to minimize air (convection) currents near critical components. Enclose either the parts with significant temperature rise, or the critical parts. Conformal coating may also help.

ISOLATION FROM HEAT GENERATORS

It is possible to thermally isolate critical areas on the PCB. Regions with little or no metal act like a good thermal insulator. Signals that need to cross these regions can be sent through series resistors, which will also act as poorly conducting thermal elements.

Place heat sources as far away from critical points as possible. Since many heat sources are in the external environment, it can be important to place these critical points far away from the edges of the PCB. Components that dissipate a lot of power should be kept far away from critical areas of the PCB.

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Low profile components will have reduced exposure to the external environment. They may have the additional advantage of reduced electrical crosstalk.

Thermal barriers, such as conformal coating and PCB enclosures, can be helpful too. They usually do not have to be added unless there are other compelling reasons to do so.

Slow Temperature Changes

In some applications, sudden changes in thermoelectric voltages can also be a concern.

Avoid power-up and power-down thermal transient problems by minimizing the currents drawn during these times. Also, reducing the times can help.

Quick changes in voltages at heavy loads can be another source of concern. If the load cannot be made lighter, then isolation is usually the best approach to solving this problem.

CURING THERMOELECTRIC VOLTAGE EFFECTS

This section focuses on methods that minimize the effects of a given temperature gradient. They can be powerful aids in improving a design because they tend to be low cost.

Metallurgy

Critical points, that need to have the same total thermoelectric voltage, should use the same conductive material. For example, the inputs to an op amp should connect to the same materials. The PCB traces will match well, but components with different constructions may be a source of trouble.

It is possible to find combinations of metals and solders that have low Seebeck coefficients. While this obviously reduces voltage errors, this can be complicated and expensive to implement in manufacturing.

Following Contour Lines

Place critical components so that their current flow follows constant temperature contour lines; this minimizes their thermoelectric voltages. Figure 5 shows an inverting amplifier that will be used to illustrate this concept; R_N , R_G and R_F are the critical components in this circuit.

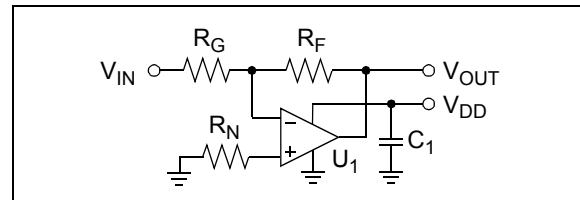


FIGURE 5: Inverting Amplifier.

Figure 6 shows one implementation of this concept. Constant temperature contour lines become reasonably straight when they are far from the heat source. Placing the resistors in parallel with these lines minimizes the temperature drop across them.

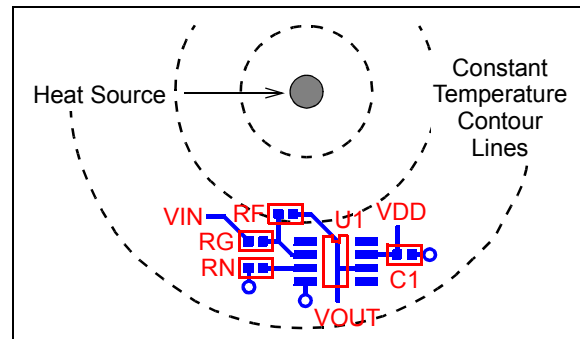


FIGURE 6: Resistors Aligned with Contour Lines.

The main drawback to this technique is that the contour lines change when the external thermal environment changes. For instance, picking up a PCB with your hands adds heat to the PCB, usually at locations not accounted for in the design.

Cancellation of Thermoelectric Voltages

It is possible to cancel thermoelectric voltages when the temperature gradient is constant. Several examples will be given to make this technique easy to understand.

TRADITIONAL OP AMP LAYOUT APPROACH

Figure 7 shows a non-inverting amplifier that needs to have the resistors' thermoelectric voltage effect minimized. The traditional approach is to lay out the input resistors (R_N and R_G) close together, at equal distances from the op amp input pins and in parallel.

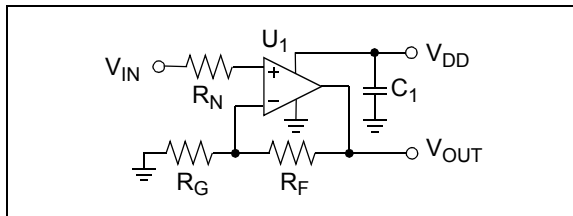


FIGURE 7: Non-inverting Amplifier.

Figure 8 shows one layout that follows the traditional approach, together with a circuit diagram that includes the resulting thermoelectric voltages (V_{THx} and V_{THy}). V_{THx} is positive on the right side of a horizontally oriented component (e.g., R_N). V_{THy} is positive on the top side of a vertically oriented component (e.g., R_F).

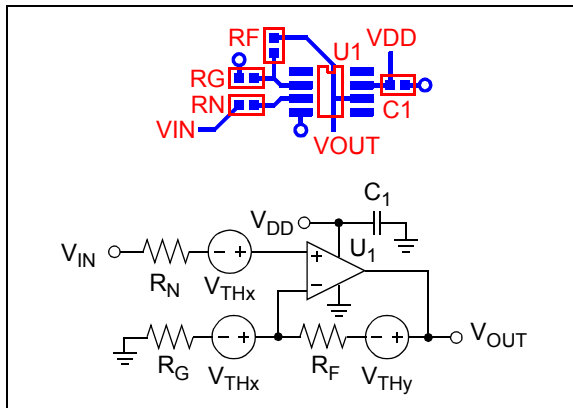


FIGURE 8: One Possible Layout (not recommended) and its Thermoelectric Voltage Model.

The output has a simple relationship to the inputs (V_{IN} and the three V_{THx} and V_{THy} sources):

EQUATION 2:

$$G_N = 1 + R_F/R_G$$

$$V_{OUT} = (V_{IN} + V_{THx})G_N - V_{THx}(G_N - 1) + V_{THy}$$

$$= V_{IN}G_N + V_{THx} + V_{THy}$$

When the gain (G_N) is high, the thermoelectric voltage contributes little to the output error. This layout may be good enough in that case. Notice that the cancellation between R_N and R_G is critical to good performance.

When the gain is low, or the very best performance is desired, this layout needs improvement. The following sections give guidance that helps achieve this goal.

SINGLE RESISTOR SUBSTITUTIONS

A single resistor on a PCB will produce a thermoelectric voltage, as discussed before. Replacing that resistor with two resistors that are properly aligned will cancel the two resulting thermoelectric voltages.

Figure 9 shows the original resistor and its model on the top, and a two series resistor substitution and its model on the bottom.

The original resistor has a thermally induced voltage V_{THx} that is based on the temperature gradient in the x-direction (horizontal).

The two resistors on the bottom have thermally induced voltages V_{THy} that are based on the temperature gradient in the y-direction (vertical); they are equal because the temperature gradient is constant and the resistor lengths are equal. Due to their parallel alignment, these voltages cancel; the net thermally induced voltage for this combination (as laid out) is zero.

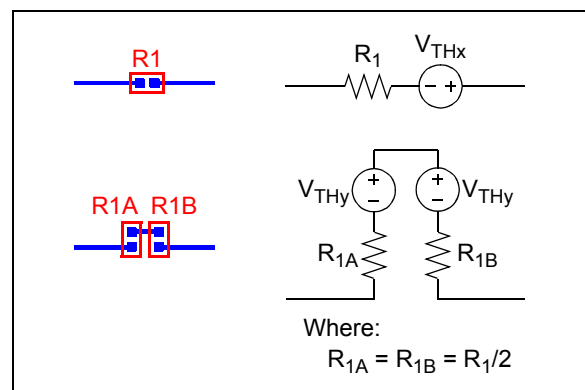


FIGURE 9: Series Resistor Substitution.

Note: The orientation of these two resistors (R_{1A} and R_{1B}) is critical to canceling the thermoelectric voltages.

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Figure 10 shows the original resistor and its model on the top, and a two parallel resistor substitution and its model on the bottom.

The original resistor has a thermally induced voltage V_{THx} that is based on the temperature gradient in the x-direction (horizontal).

The two resistors on the bottom have thermally induced voltages V_{THy} that are based on the temperature gradient in the y-direction (vertical); they are equal because the temperature gradient is constant and the resistor lengths are equal. Due to their orientation, and because $R_{1A} = R_{1B}$, these voltages produce currents that cancel. The net thermally induced voltage for this combination (as laid out) is zero.

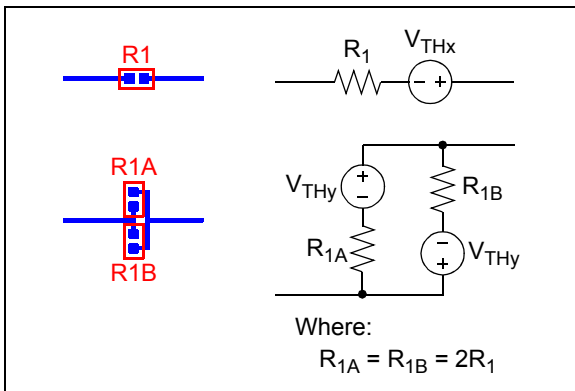


FIGURE 10: Parallel Resistor Substitution.

NON-INVERTING AMPLIFIER

Figure 11 shows a non-inverting amplifier. We will start with the layout in Figure 12 (previously shown in Figure 6). The resistor R_F is horizontal so that all of the thermoelectric voltages may be (hopefully) cancelled. The model shows how the thermoelectric voltages modify the circuit.

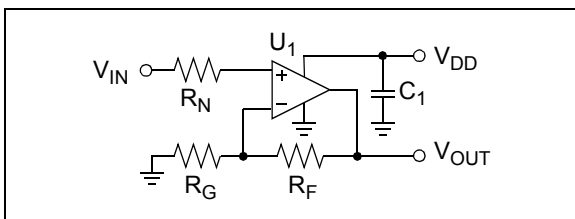


FIGURE 11: Non-inverting Amplifier.

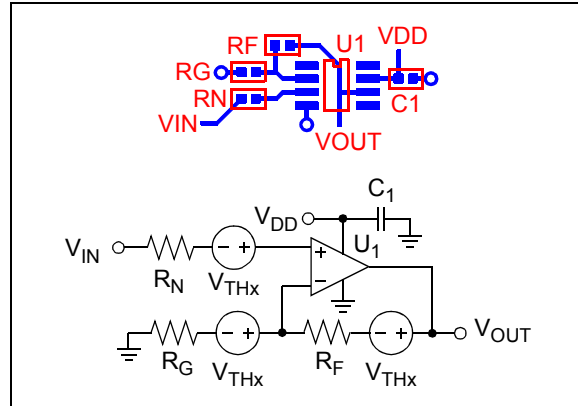


FIGURE 12: First Layout (not recommended) and its Thermoelectric Voltage Model.

The output has a simple relationship to the inputs (V_{IN} and the three V_{THx} sources):

EQUATION 3:

$$G_N = 1 + R_F/R_G$$

$$V_{OUT} = (V_{IN} + V_{THx})G_N - V_{THx}(G_N - 1) + V_{THx}$$

$$= V_{IN}G_N + 2V_{THx}$$

When the gain (G_N) is high, the thermoelectric voltage's contribution to the output error is relatively small. This layout may be good enough in that case. Notice that the cancellation between R_N and R_G is critical.

We have a better layout shown in Figure 13. Recognizing that subtracting the last term in the V_{OUT} equation (middle equation in Equation 3) completely cancels the thermoelectric voltages, the resistor R_F was oriented in the reverse direction.

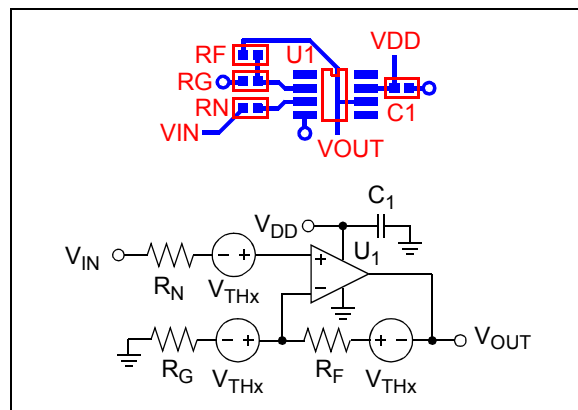


FIGURE 13: Second Layout and its Thermoelectric Voltage Model.

With the reversed direction for R_F , the output voltage is now:

EQUATION 4:

$$G_N = 1 + R_F/R_G$$

$$V_{OUT} = (V_{IN} + V_{THx})G_N - V_{THx}(G_N - 1) - V_{THx}$$

$$= V_{IN}G_N$$

The cancellation between R_N and R_G is critical to this layout; the change to R_F 's position is not as important.

INVERTING AMPLIFIER

Inverting amplifiers use the same components as non-inverting amplifiers, so the resistor layout is the same; see [Figure 14](#).

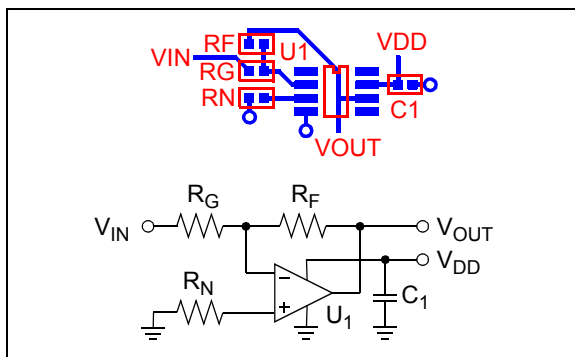


FIGURE 14: Inverting Amplifier.

DIFFERENCE AMPLIFIER

[Figure 15](#) shows a difference amplifier. This topology has an inherent symmetry between the non-inverting and inverting signal paths, which lends itself to cancelling the thermoelectric voltages. [Figure 16](#) shows the layout and its model.

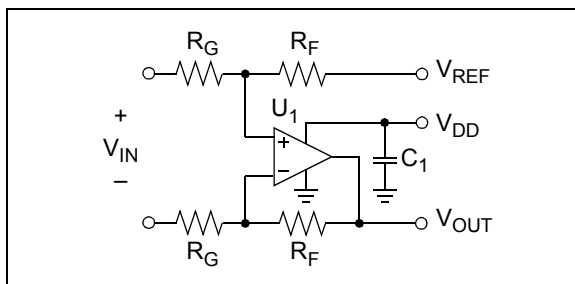


FIGURE 15: Difference Amplifier.

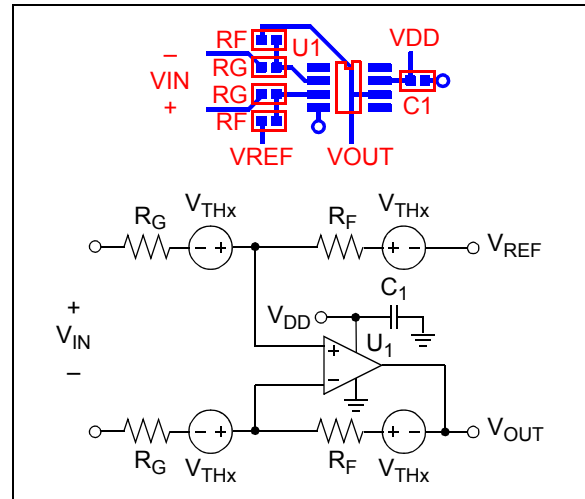


FIGURE 16: Difference Amplifier Layout and its Thermoelectric Voltage Model.

The output has a simple relationship to the inputs (V_{IN} , V_{REF} and the four V_{THx} sources):

EQUATION 5:

$$G = R_F/R_G$$

$$V_{OUT} = (V_{IN} + V_{THx} - V_{THx})G$$

$$+ (V_{REF} + V_{THx} - V_{THx})$$

$$= V_{IN}G + V_{REF}$$

INSTRUMENTATION AMPLIFIER INPUT STAGE

[Figure 17](#) shows an instrumentation amplifier input stage, which is sometimes used to drive the input of a differential ADC. While this is a symmetrical circuit, achieving good thermoelectric voltage cancellation on the PCB presents difficulties. It is best to use a dual op amp, so the R_F resistors have to be on both sides of the op amp, while R_G connects both sides; the distances between resistors are too large to be practical (thermal gradient is not constant).

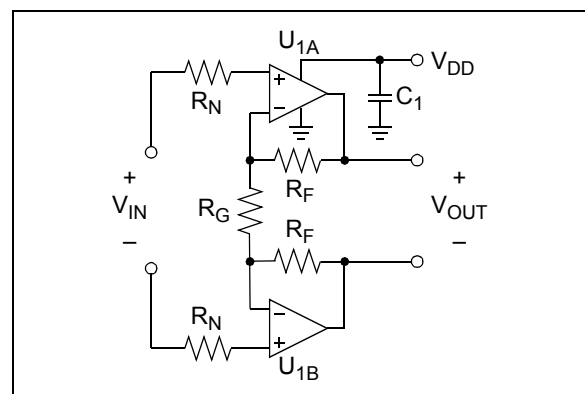


FIGURE 17: Instrumentation Amplifier Input Stage (not recommended).

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The solution to this problem is very simple; split R_G into two equal series resistors so that we can use the non-inverting layout (see [Figure 13](#)) on both sides of the dual op amp. Each side of this amplifier will cancel its thermoelectric voltages independently; this is shown in [Figure 18](#) and [Figure 19](#).

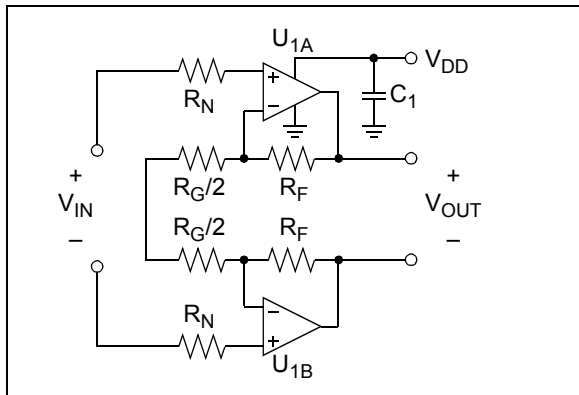


FIGURE 18: Instrumentation Amplifier Input Stage.

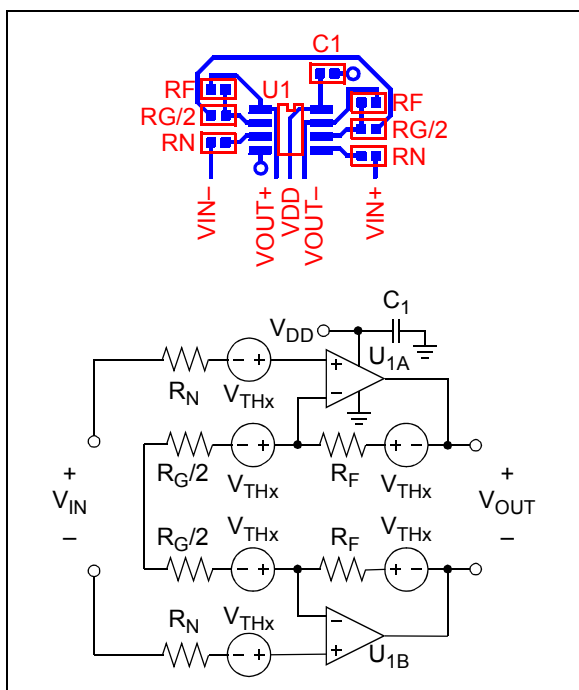


FIGURE 19: Instrumentation Amplifier Input Stage Layout and its Thermoelectric Voltage Model.

The V_{THx} sources cancel, for the reasons already given, so the differential output voltage is simply:

EQUATION 6:

$$G = 1 + 2R_F/R_G$$

$$V_{OUT} = V_{IN}G$$

MODIFICATIONS FOR NON-CONSTANT TEMPERATURE GRADIENTS

Temperature gradients are never exactly constant. One cause is the wide range of thermal conductivities (e.g., traces vs. FR4) on a PCB, which causes complex temperature profiles. Another cause is that many heat sources act like point sources, and the heat is mainly conducted by a two dimensional object (the PCB); the temperature changes rapidly near the source and slower far away.

Non-constant temperature gradients will cause the temperature profile to have significant curvature, which causes all of the previous techniques to have less than perfect success. Usually, the curvature is small enough so that those techniques are still worth using. Sometimes, additional measures are needed to overcome the problems caused by the curvature.

One method is to minimize the size of critical components (e.g., resistors). If we assume that temperature has a quadratic shape, then using components that are half as long should reduce the non-linearity error to about one quarter the size.

Another method is to keep all heat sources and sinks far away from the critical components. This makes the contour lines straighter.

The contour lines can be deliberately changed in shape. Using a ground plane (also power planes) to conduct heat away from the sources helps equalize the temperatures, which reduces the non-linear errors. Adding guard traces or thermal heat sinks that surround the critical components also help equalize the temperatures.

We can modify the sizes of the critical components so that the cancellation becomes closer to exact. In order to match resistors, for instance, we need to make sure that the temperature change across each of the matched resistors is equal; see [Figure 20](#) for an illustration.

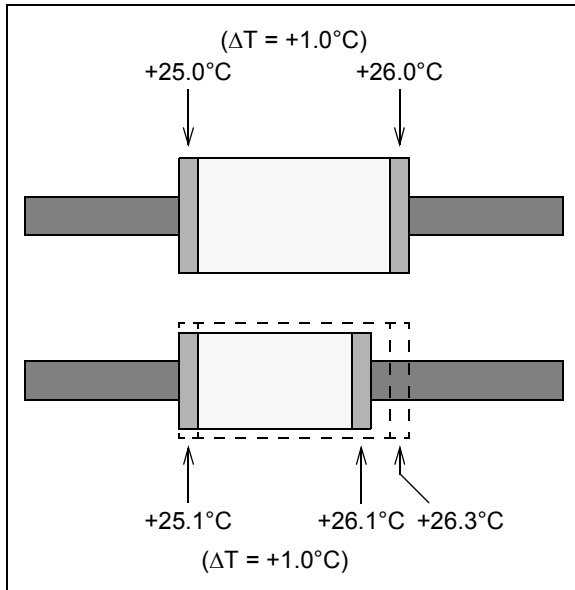


FIGURE 20: Example of Mismatching the Component Sizes.

MEASUREMENT OF TEMPERATURE RELATED QUANTITIES

While the techniques previously shown are a great help in producing an initial PCB layout, it is important to verify that your design functions as specified. This section includes methods for measuring the response of individual components and of a PCB. With this information, it is possible to make intelligent design tweaks.

TEMPERATURE

There are many ways to measure temperature [4, 5, 6]. We could use thermocouples, RTDs, thermistors, diodes, ICs or thermal imagers (infrared cameras) to measure the temperature.

Figure 21 shows a circuit based on the MCP9700 IC temperature sensor. Because all of the components draw very little current, their effect on PCB temperature will be minimal. There is enough filtering and gain to make V_{OUT} easy to interpret. This circuit can be built on a very small board of its own, which can be easily placed on top of the PCB of interest.

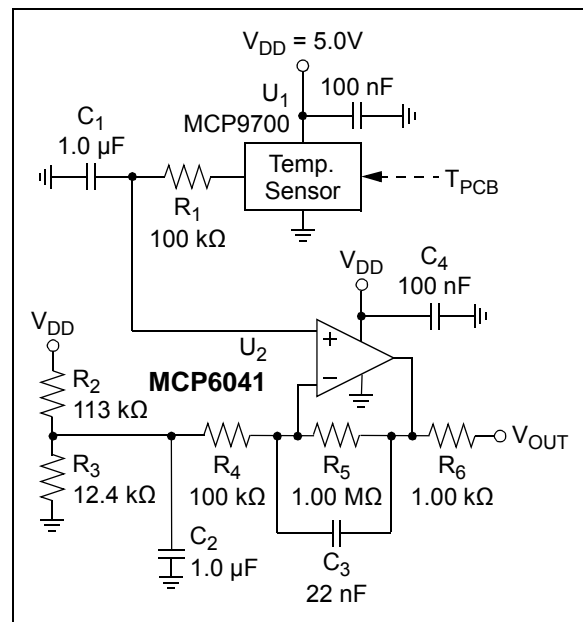


FIGURE 21: IC Temperature Sensor Circuit.

The MCP9700 outputs a voltage of about 500 mV plus 10.0 mV/°C times the board temperature (T_{PCB} , in °C). The amplifier provides a gain of 10 V/V centered on 500 mV (when $V_{DD} = 5.0V$), giving:

EQUATION 7:

$$V_{OUT} = (500 \text{ mV}) + T_{PCB}(100 \text{ mV}/^{\circ}\text{C})$$

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Since the MCP9700 outputs a voltage proportional to temperature, V_{OUT} needs to be sampled by an ADC that uses an absolute voltage reference.

The absolute accuracy of this circuit does not support our application, so it is important to calibrate the errors. Leave the PCB in a powered-off state (except for the temperature sensor) for several minutes. Measure V_{OUT} at each point, with adequate averaging. The changes in V_{OUT} from the calibration value represents the change in T_{PCB} from the no power condition.

THERMAL GRADIENTS

To measure thermal gradients, simply measure the temperature at several points on the PCB. The gradient is then the change in temperature divided by the distance between points. More points give better resolution on the gradient, but reduce the accuracy of the numerical derivative.

PACKAGE THERMAL RESISTANCE

The way to estimate the temperature (T in $^{\circ}\text{C}$) of a component is to multiply its dissipated power (P in W) by the package thermal resistance (θ_{JA} in $^{\circ}\text{C}/\text{W}$). This helps establish temperature maximum points.

To measure θ_{JA} , when it is not given in a data sheet, place the temperature sensor at the IC (usually, a thermocouple between the package and the PCB). Insert a small resistor in the supply to measure the supply current when on (I_{DD} in A). Measure the change in temperature (ΔT in $^{\circ}\text{C}$) between the off and on conditions, supply voltage (V_{DD} in V) and I_{DD} . Then,

EQUATION 8:

$$\theta_{JA} = \frac{\Delta T}{V_{DD} I_{DD}}$$

THERMOELECTRIC VOLTAGES

The easiest way to measure thermoelectric voltages is to thermally imbalance a difference amplifier circuit. The thermoelectric voltages have a polarity that adds (instead of cancelling) in [Figure 22](#) (compare to [Figure 16](#)). The differential input voltage is zero, and the resistors are larger to emphasize the thermoelectric voltages.

The large resistor on the right of the layout can be used to generate heat, causing a horizontal temperature gradient at the resistors R_G and R_F . The gain (G) is set high to make the measurements more accurate. The thermoelectric voltage (V_{THx}) across one resistor is:

EQUATION 9:

$$G = R_F/R_G$$

$$V_{THx} = \frac{V_{OUT} - V_{REF}}{2G + 2}$$

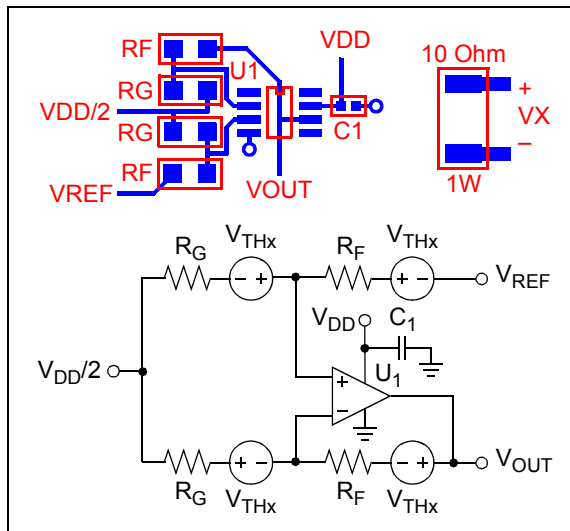


FIGURE 22: Difference Amplifier with Deliberately Unbalanced Thermoelectric Voltages and Heat Generating Resistor.

We can also place a short across one component, of a matched pair, with a copper trace on the PCB. [Figure 23](#) shows a non-inverting amplifier layout that shorts R_N (with a copper trace) to unbalance the thermoelectric voltages. It also connects the two inputs together, and uses larger resistors, to simplify measurements ($V_{OUT} = V_{DD}/2$, ideally). The short is easily removed from the PCB.

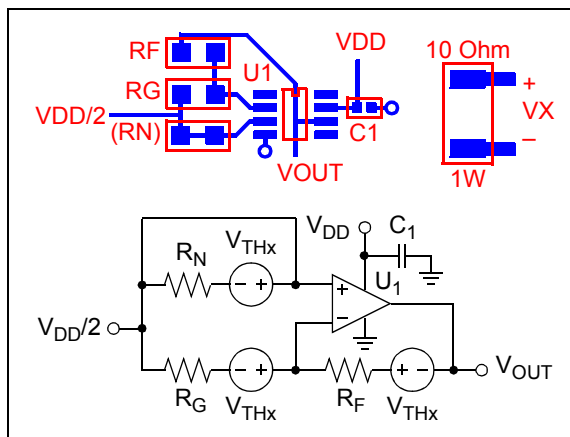


FIGURE 23: Shorted Resistor (R_N) that Unbalances Thermoelectric Voltages.

With the unbalance, we now have the thermoelectric voltage:

EQUATION 10:

$$G_N = 1 + R_F/R_G$$

$$V_{THx} = \frac{V_{OUT} - V_{DD}/2}{-G_N}$$

TROUBLESHOOTING TIPS AND TRICKS

Using a strip chart to track the change in critical DC voltages over time helps locate the physical source of the errors. Not only can it show how large the change is between two different thermal conditions (e.g., on and off), but it shows the time constants of these shifts. They can be roughly divided into the following three categories:

- Time constant $\ll 1$ s, within component (e.g., thermal crosstalk within an op amp)
- Time constant ≈ 1 s, single component (e.g., in an eight lead SOIC package)
- Time constant $\gg 1$ s, PCB and its environment

To quickly and easily change the temperature at one location on a PCB, do the following. Use a clean drinking straw to blow air at the location (component) of interest. Use a piece of paper to re-direct the airflow away from other nearby components. When troubleshooting, the paper can be used to divide a PCB area in half to help locate the problem component. This approach does not give exact numbers, but can be used to quickly find problem components on a PCB.

You can use a heat sink (with electrically insulating heat sink compound) to reduce the temperature difference between two critical points on your PCB. The greater the area covered at both ends of the heat sink, the quicker and better this thermal "short" will work.

LEAKAGE CURRENTS

Leakage currents cause voltage drops when they flow through either resistors or parasitic resistances. This section focuses on parasitic resistances presented by the PCB: surface resistance and bulk (through the dielectric) resistance.

Leakage currents cause voltage ramps when they flow into a capacitor. Common examples are the gain capacitor of a transimpedance amplifier (see [Figure 32](#)) and the non-inverting input of an op amp with no DC path to ground (not recommended).

Op amp leakage (bias) currents are discussed in [2].

High Impedance Sources

High impedance signal sources are susceptible to errors caused by leakage currents. These sources are usually modeled as a current source with a high parallel resistance (a Norton model):

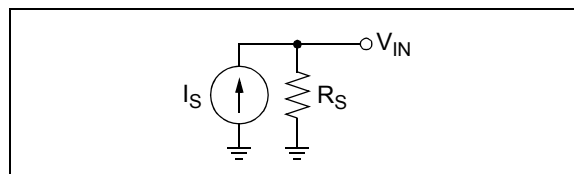


FIGURE 24: *Norton Source Model.*

One sensor that is modeled as a Norton current source is the photodiode [1]. A common op amp circuit used for photocurrent measurements is the transimpedance amplifier (see [Figure 32](#)).

Sometimes, high impedance sources are modeled as a voltage source with a high series resistance (a Thevenin model):

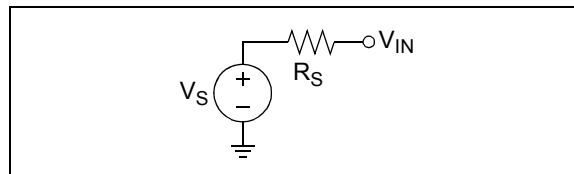


FIGURE 25: *Thevenin Source Model.*

The pH electrode [1] is one example with a Thevenin source. A common op amp implementation is a non-inverting amplifier.

PCB Surface Leakage

PARASITIC SURFACE RESISTANCES

Surface contamination on a PCB creates resistive paths for leakage currents. These leakage currents can cause appreciable voltage shifts, even in well-designed circuits. The contamination can be humidity (moisture), dust, chemical residue, etc.

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On a PCB, leakage currents flow on the surface, to a sensitive node (high resistance), from nearby bare metal objects (including traces) at a different voltage.

To model sensitivity to surface contamination in your circuit, add resistors between the high impedance node and other nearby nodes. For example, [Figure 26](#) shows an amplifier circuit with a Thevenin source (V_S and R_S). Since R_S is high and the amplifier's input is high impedance, V_{IN} is a high impedance node. Parasitic resistances (R_{P1} to R_{P4}) are connected to all other (nearby) voltage nodes (traces on a PCB), including ground. R_{P1} to R_{P4} are open-circuited for most design work. For leakage current design calculations, they take on high resistance values (usually one at a time).

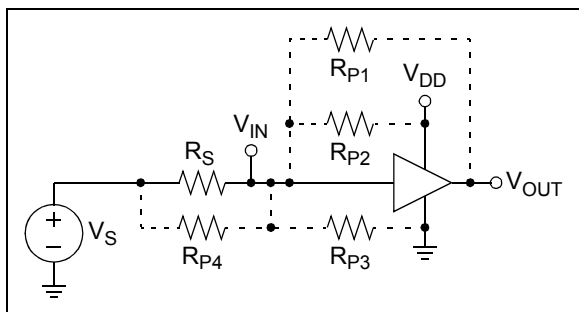


FIGURE 26: Thevenin Source and Parasitic Leakage Resistances.

[Figure 27](#) shows an amplifier circuit with a Norton source.

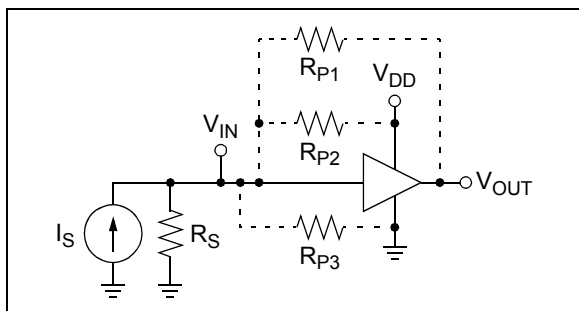


FIGURE 27: Norton Source and Parasitic Leakage Resistances.

The parasitic resistor values (R_P) depend on your PCB layout. For a typical layout, with today's geometries (traces are close and short) and materials, we have:

- $R_P \sim 1000 \text{ G}\Omega$, low humidity and contamination
- $R_P \sim 1 \text{ G}\Omega$, high humidity and contamination

These R_P values need to be modified for atypical geometries; see [Appendix B: "PCB Parasitic Resistance"](#). These R_P values also need to be modified for the worst case conditions for your application. Measurements in your conditions, and with your PCB layout, will give better estimates of R_P .

CLEANING

A standard PCB clean step helps minimize surface contamination, but may not eliminate the problem. An additional cleaning step, using isopropyl alcohol, is needed to clean the residue left by some PCB cleaning solvents. This can then be blown dry using compressed air (with an in-line moisture trap).

COATING

In order to maintain the PCB cleanliness after the initial clean, you may coat the PCB surface. The coating needs to be a barrier to moisture and other contaminants; solder mask, epoxy and silicone rubber are examples.

The coating will have internal (bulk) leakage currents; this effect needs to be evaluated for your design.

GUARD RINGS

Guard rings surrounding critical signal traces, when properly applied, can significantly reduce PCB surface leakage currents into critical (high resistance) nodes.

These guard rings have no solder mask so that the leakage currents flow into them, instead of into the sensitive trace. The guard ring is biased at the same voltage as the sensitive node; it needs to be driven by a low impedance source.

Guard rings increase the capacitance at critical nodes. Since they are driven by low impedance sources, these capacitances have little effect on performance.

Unity Gain Buffer

[Figure 28](#) shows a unity gain buffer with a guard ring. This guard ring is biased by V_{OUT} and protects (surrounds) the op amp's non-inverting input (and all top metal connected to it) on the PCB surface. The diagram is for surface mount components only. R_N is an 0805 SMD to give sufficient clearance for the guard ring trace between its pads.

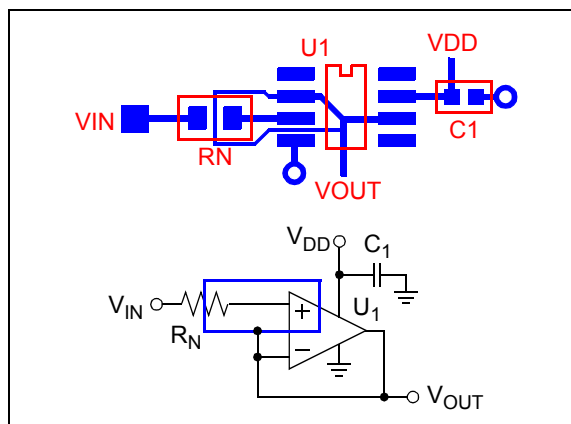


FIGURE 28: Unity Gain Buffer with Guard Ring.

The parasitic resistances are connected as shown in [Figure 29](#). R_{P2} injects current into U_1 's non-inverting input (the high impedance node). The other parasitic resistors inject current into the guard ring, which is driven by V_{OUT} ; they do not affect the performance.

The voltage across R_{P2} is U_1 's offset voltage (V_{OS}), so the leakage current is greatly reduced. For instance, if $V_{OS} \leq \pm 2$ mV and the voltage without the guard ring is 2V, the leakage current would be reduced by a factor of about 1000.

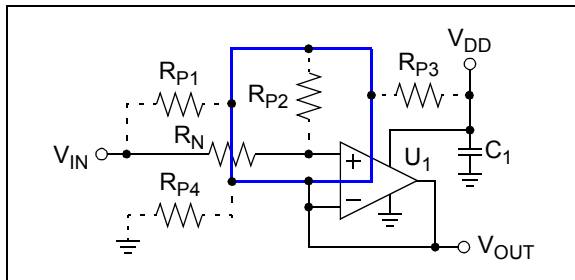


FIGURE 29: *Equivalent Circuit for Unity Gain Buffer with Guard Ring.*

One example of an application that sometimes uses unity gain op amps are pH meters. In that case, however, both V_{IN} and R_N are located off the PCB; the guard ring only needs to surround U_1 's non-inverting input.

Non-inverting Gain Amplifier

[Figure 30](#) shows a non-inverting gain amplifier with a guard ring. This guard ring is biased by V_{OUT} . R_F and R_G ; it protects (surrounds) the op amp's non-inverting input (and all top metal connected to it) on the PCB surface. R_F and R_G are low impedance, to drive the guard ring properly. R_N is a low valued resistor that cancels thermojunction voltage effects, but has little effect on bias current errors (e.g., $I_B R_N \ll \pm 1$ mV).

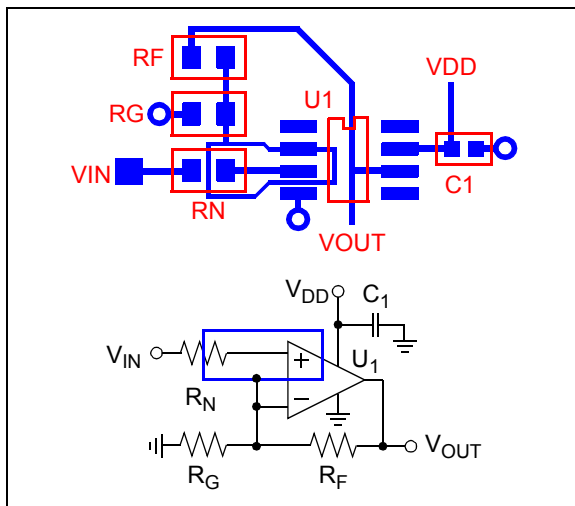


FIGURE 30: *Non-inverting Gain Amplifier with Guard Ring.*

The parasitic resistances are connected as shown in [Figure 31](#). Similar to the Unity Gain Buffer in the last section, U_1 's offset voltage (V_{OS}) is across R_{P2} , which greatly reduces its leakage current. The other parasitic resistances are driven by V_{OUT} , R_F and R_G ; they do not affect the performance. The leakage current is typically reduced by a factor of about 1000.

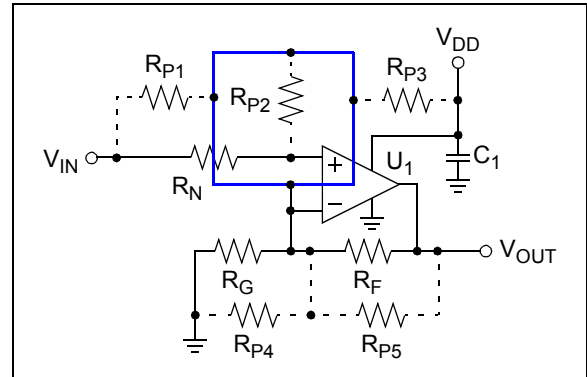


FIGURE 31: *Equivalent Circuit for Non-inverting Amplifier with Guard Ring.*

Transimpedance Amplifier

[Figure 32](#) shows a photo-diode at the input of a transimpedance amplifier, with a guard ring. This guard ring is biased at ground; it protects (surrounds) the op amp's inverting input (and all top metal connected to it) on the PCB surface. R_F is high valued for the DC gain (V_{OUT}/I_{D1}).

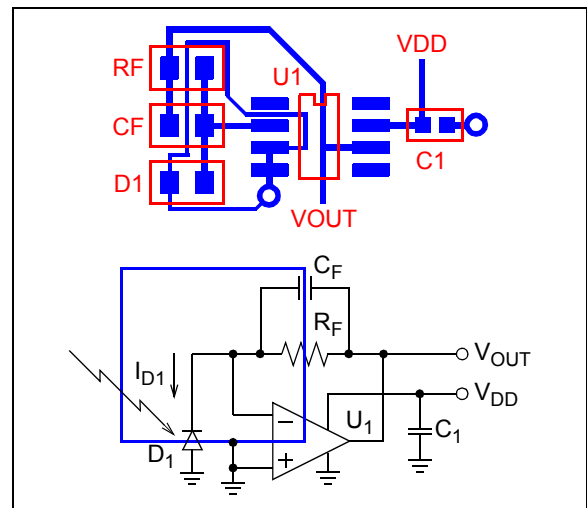


FIGURE 32: *Photo-diode and Transimpedance Amplifier, with Guard Ring.*

The parasitic resistances are connected as shown in [Figure 33](#). Similar to the Non-inverting Gain Amplifier in the last section, U_1 's offset voltage (V_{OS}) is across R_{P1} , which greatly reduces its leakage current. The other parasitic resistances are connected to ground; they do not affect the performance. The leakage current is typically reduced by a factor of about 1000.

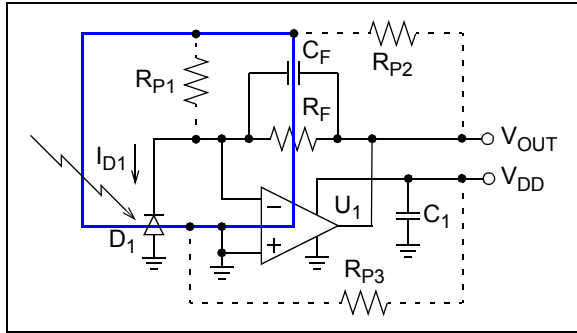


FIGURE 33: *Equivalent Circuit for Photodiode and Transimpedance Amplifier, with Guard Ring.*

Guard Rings on Both PCB Surfaces

For op amps in through-hole packages (e.g., PDIP), guard rings are needed on both top and bottom surfaces. The same design principles apply to both surfaces.

Any jumper traces (via to other surface, trace and via back to the original surface), connected to traces with guard rings, also need guard rings around the jumper traces. It is better, when possible, to avoid jumper traces for critical nodes.

PCB Bulk Leakage

The dielectric material used in a PCB (e.g., FR4) is an insulator. Its resistance to leakage currents through the bulk (the dielectric) is described by its volume resistivity (ρ_V). ρ_V values vary considerably, depending on the dielectric and on ambient conditions.

Usually, bulk leakage currents are much smaller than surface leakage currents; they can be neglected in many designs. Designs that minimize surface leakage currents, however, may be affected by bulk currents.

Example 1 shows one example of how bulk leakage currents occur. Two traces run in parallel and are separated by the dielectric. The leakage current between the traces, flowing through the dielectric, is modelled by a parasitic resistor (see R_{P1} in **Figure 34**).

EXAMPLE 1: PARALLEL TRACES, OPPOSITE SURFACES

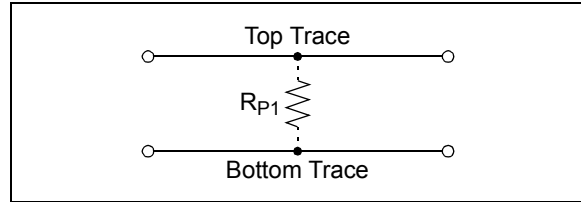
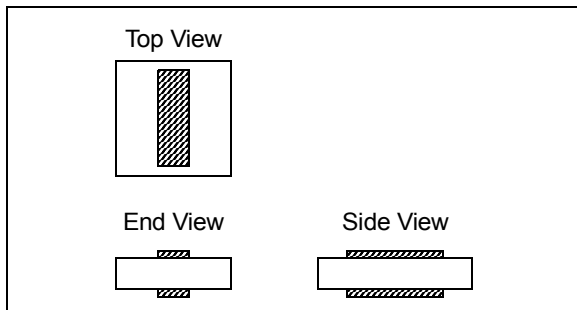


FIGURE 34: *Equivalent Circuit for Parallel Traces, Opposite Surfaces.*

Any two metal areas on the PCB (on a surface or buried in an inner layer), at different potentials, will have a leakage current between them. The value of the parasitic (bulk) resistance depends on:

- The geometry of the areas
 - The distance between
 - The cross sectional area seen by the current
- Nearby metal objects (e.g., a guard ring) that modify the current flow path
- The volume resistivity (ρ_V)
 - Dielectric material
 - Exposure to chemicals (e.g., water)

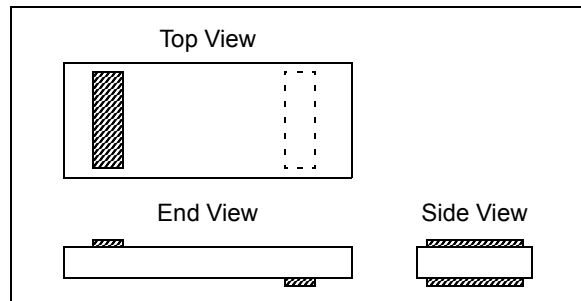
The following discussion shows simple techniques to minimize these leakage currents. See **Appendix B: “PCB Parasitic Resistance”** for ways to estimate bulk leakage currents.

SEPARATION

Moving traces to the surfaces, from inner layers, increases the distance between them (e.g., **Example 1**).

Example 2 shows two parallel traces, with a distance separating them. This extra distance increases the parasitic resistance.

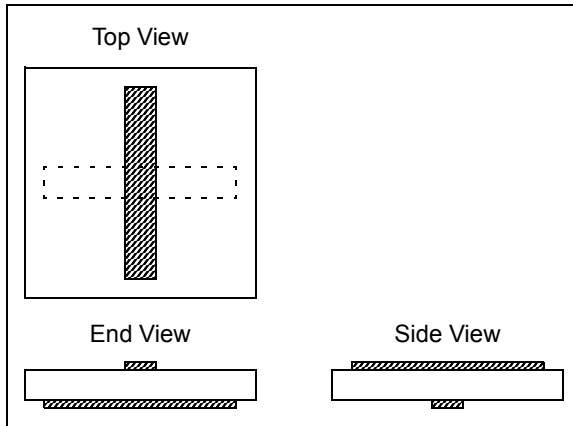
EXAMPLE 2: TWO PARALLEL TRACES, WITH OFFSET



CROSSED TRACES

When two traces must cross, place them on opposite surfaces and in normal directions to minimize the parasitic resistance; see [Example 3](#).

EXAMPLE 3: TWO NORMAL TRACES



GUARD RINGS

[Example 4](#) shows a trace on the left (node 1), a guard ring (node 2) and a sensitive trace (node 3). The guard ring provides a low resistance path that redirects some of the current between node 1 and node 3 to itself. R_{PB2} in [Figure 35](#) acts as an attenuator to the input voltage (V_1). When $V_2 \approx V_3$, the parasitic current (into V_3) is significantly reduced.

EXAMPLE 4: TWO PARALLEL TRACES, WITH GUARD RING

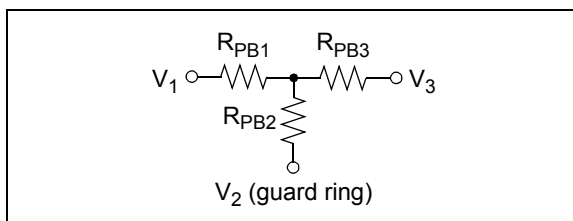
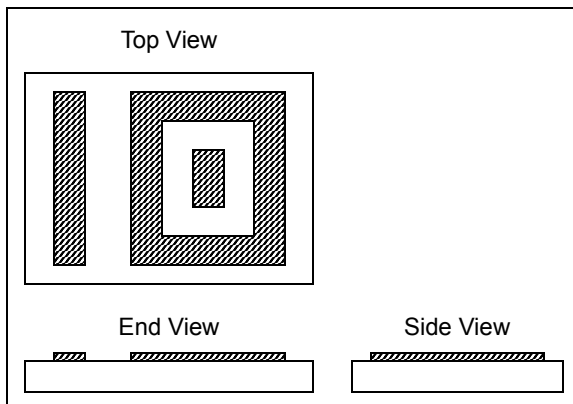


FIGURE 35: *Equivalent Circuit for Two Parallel Traces, With Guard Ring.*

GUARD PLANE

[Example 5](#) shows a trace on the left (node 1), a guard plane (node 2) and a sensitive trace (node 3). The guard plane behaves similar to a guard ring, except that it forms a distributed attenuator to the input voltage (see [Figure 36](#)); this attenuation can be much greater.

EXAMPLE 5: TWO PARALLEL TRACES, WITH GUARD PLANE

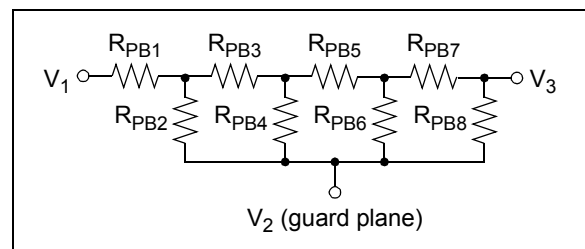
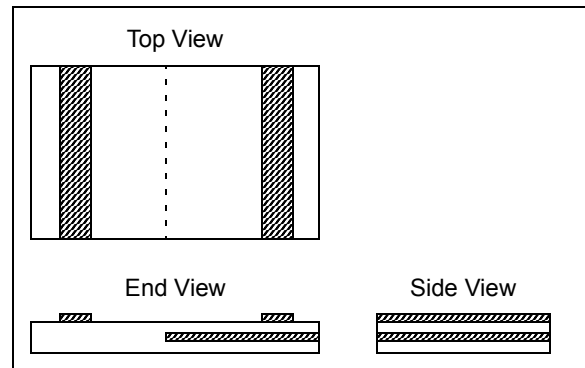


FIGURE 36: *(Lumped) Equivalent Circuit for Two Parallel Traces, With Guard Plane.*

DIELECTRIC MATERIAL

Changing the dielectric material changes its bulk resistivity (ρ_V) and susceptibility to humidity. For designs that need exceptional performance, this is an option worth exploring.

MOISTURE CONTROL

When a dielectric is exposed to moisture for an extended period of time, it can become wet. This reduces its bulk resistivity (ρ_V).

Measures to control exposure to moisture reduce this effect. One possibility is the use of coatings.

ISOLATING SENSITIVE NODES

Another way to minimize PCB leakage currents is to isolate sensitive nodes (wires, package pins, etc.) from the board (i.e., not touching).

One approach is to use teflon stand-offs. This has technical advantages, but can be costly to implement.

Another approach is to keep sensitive nodes in the air. Bending package leads and routing holes in the PCB are possible techniques to accomplish this.

OTHER TIPS

This section discusses other effects and design tips.

Packages

IC packages contribute to leakage currents. Pins that are close together (fine pitch) will see greater leakage currents, due to dust and shorter leakage paths. The package itself will have bulk leakage, which depends on its chemistry.

Piezoelectric Effect

Some capacitors accumulate extra charge from mechanical stress (a variable capacitor), creating a DC shift. Some ceramic capacitors (not all) suffer from this effect. Minimize stresses with acoustic noise reduction techniques, and by making the PCB assembly more rigid.

Triboelectric Effect

Mechanical friction can cause charges to accumulate (a variable capacitor), causing a DC shift. Air flow over a PCB is one source of mechanical friction. Flexing wires and coax cables excessively can also cause this to happen. Shield against air flow, and make bends in wiring with a large radius. For remote sensors, use low noise coax or triax cable.

Contact Potential

Sometimes, for convenience on the bench, a PCB has sockets for critical components (e.g., an op amp). While these sockets make it easy to change components, they cause significant DC errors in high precision designs.

The problem is that the socket and the IC pins are made of different metals, and are mechanically forced into contact. In this situation, there is a (contact) voltage potential developed between the metals (the Volta effect). Physicists explain this phenomenon through the difference between their work functions. In our bench tests of our auto-zeroed op amps, we saw voltage potentials of $\pm 1 \mu\text{V}$ to $\pm 2 \mu\text{V}$ due to the IC socket.

The solution is very simple; do not use sockets for critical components. Instead, solder all critical components to the PCB.

DESIGN EXAMPLE

This section goes over the thermal design of a thermocouple PCB available from Microchip. This PCB has the following descriptors:

- MCP6V01 Thermocouple Auto-Zeroed Reference Design
- 104-00169-R2
- MCP6V01RD-TCPL

The application of this PCB is discussed in detail in reference [7].

Circuit Description

Figure 37 shows the general functionality of this design (the schematic is shown in Figure A-1).

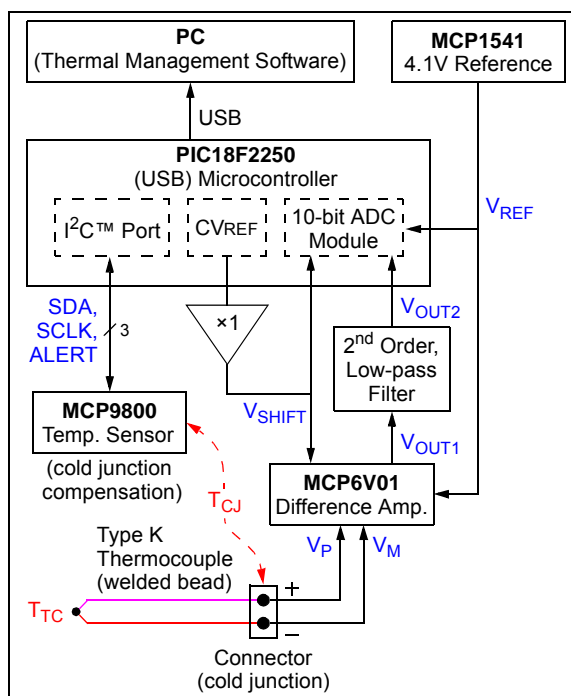


FIGURE 37: Thermocouple Circuit's Block Diagram.

The (type K) thermocouple senses temperature at its hot junction (T_{TC}) and produces a voltage at the cold junction (at temperature T_{CJ}). The conversion constant for type K thermocouples is roughly $40 \mu\text{V}/^\circ\text{C}$. This voltage ($V_P - V_M$) is input to the Difference Amplifier (MCP6V01).

The MCP9800 senses temperature at the Type K Thermocouple's cold junction (T_{CJ}). The result is sent to the PICmicro microcontroller via an I²C™ bus. The firmware corrects the measured temperature for T_{CJ} .

The difference amplifier uses the MCP6V01 auto-zeroed op amp to amplify the thermocouple's output voltage. The V_{REF} input shifts the output voltage down so that the temperature range includes -100°C . The V_{SHIFT} input shifts the output voltage, using a

digital POT internal to the microcontroller (CVREF), so that the temperature range is segmented into 16 smaller ranges; this gives a greater range (-100°C to +1000°C) with reasonable accuracy.

The MCP1541 provides an absolute reference voltage because the thermocouple's voltage depends only on temperature (not on V_{DD}). It sets the nominal V_{OUT} and serves as the reference for the ADC internal to the microcontroller.

The 2nd Order, Low-pass Filter reduces noise and aliasing at the ADC input. A double R-C filter was chosen to minimize DC errors and complexity.

CVREF is a digital POT with low accuracy and highly variable output resistance. The buffer ($\times 1$ amplifier) eliminates the output impedance problem, producing the voltage V_{SHIFT} . Since CVREF has 16 levels, we can shift V_{OUT1} by 16 different amounts, creating 16 smaller ranges; this adds 4 bits resolution to the measured results (the most significant bits). The 10 bits produced by the ADC are the least significant bits; they describe the measured values within one of the 16 different smaller ranges.

V_{SHIFT} is brought back into the PICmicro microcontroller so that it can be sampled by the ADC. This gives V_{SHIFT} values the same accuracy as the ADC ("10 bits"), which is significantly better than CVREF's accuracy. The measured value of V_{OUT2} is adjusted by this measured V_{SHIFT} value.

The overall accuracy of this mixed signal solution is set by the 10-bit ADC. The resolution is 14 bits, but the accuracy cannot be better than the ADC, since it calibrates the measurements.

PCB Layout

In the figures in this section (Figure 38 through Figure 43), the red numbers (inside the circles) point to key design choices, which are described by a list after each figure.

Figure 38 shows the top silk screen layer of the PCB designed for the MCP6V01 Thermocouple Auto-Zeroed Reference Design.

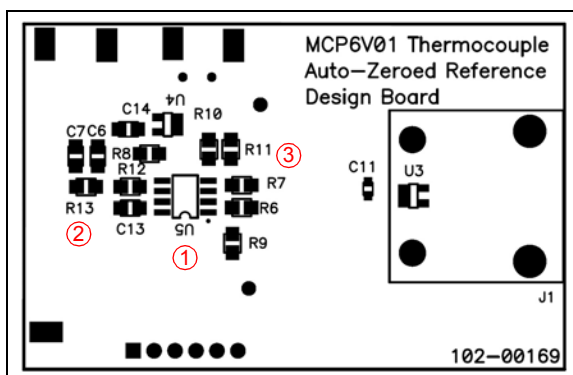


FIGURE 38: 1st Layer – Top Silk.

1. The Difference Amplifier is as close to the sensor as possible, and is on the opposite PCB surface from the PICmicro microcontroller. This minimizes electrical and thermal crosstalk between the two active devices.
2. Small resistors (0805 SMD) reduce the thermoelectric voltages, for a given temperature gradient.
3. The resistors that are a part of the Difference Amplifier play a critical role in this design's accuracy.
 - a) R6 and R7 are at the input from the thermocouple, and give a gain of 1000 V/V to V_{OUT1} . They are arranged so that their thermoelectric voltages cancel.
 - b) R9 and R10 are at the input from the range selection circuitry (V_{SHIFT}), and give a gain of 17.9 V/V to V_{OUT1} . Changing their location and orientation on the PCB might improve the performance.
 - c) R8 and R11 convert the inputs to the output voltage (V_{OUT1}). Changing their location and orientation may not improve the performance enough to be worth the trouble.

Figure 39 shows the top metal layer of the PCB. The sensitive analog and sensor circuitry is connected to this layer.

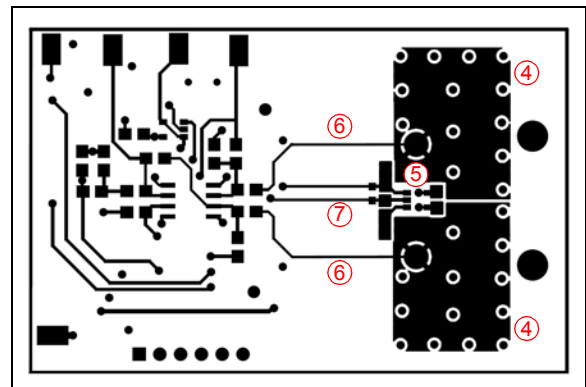


FIGURE 39: 1st Layer – Top Metal.

4. Metal fill, connected to the ground plane, minimizes thermal gradients at the cold junction connector.
5. The MCP9800 Temperature Sensor (cold junction compensation) is centered at the cold junction connector to give the most accurate reading possible.
6. Sensor traces are separated from power (top layer) and digital (bottom layer) traces to reduce crosstalk.
7. The MCP9800's power traces are kept short, straight and above ground plane for minimal crosstalk.

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Figure 40 shows the power plane. It minimizes noise conducted through the power supplies and isolates the analog and digital signals.

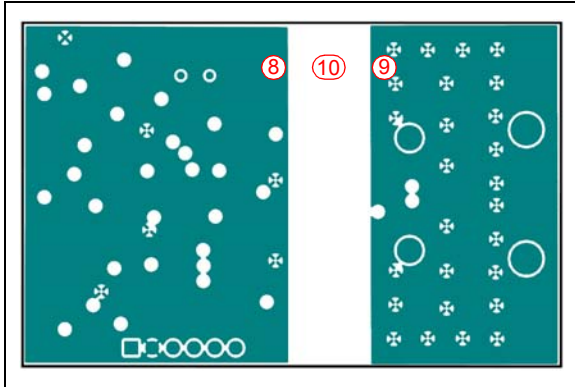


FIGURE 40: 2nd Layer – Power Plane.

8. The power plane on the left helps keep the temperature relatively constant near the auto-zeroed op amp. It also provides isolation from the microcontroller's electrical and thermal outputs.
9. The power plane on the right helps keep the temperature relatively constant near the thermocouple's cold junction and MCP9800 cold junction temperature sensor.
10. The FR4 gap provides attenuation to heat flow (a relatively high temperature drop) between the active components on the left (MCP6V01 and PIC18F2550) and the sensors on the right (thermocouple and MCP9800).

Figure 41 shows the ground plane. It also minimizes noise conducted through the power supplies and isolates the analog and digital signals.

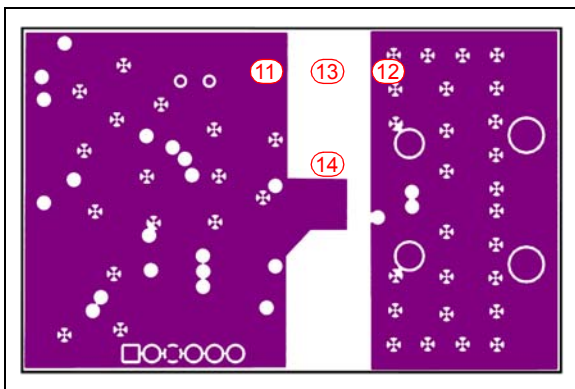


FIGURE 41: 3rd Layer – Ground Plane.

11. Same function as #8.
12. Same function as #9.
13. Same function as #10.

14. This ground plane extension provides better isolation between digital signals and the MCP9800's power supply. It also helps protect the thermocouple signal lines. However, it increases the thermal conduction between the left and right sides of the PCB.

Figure 42 shows the bottom silk layer.

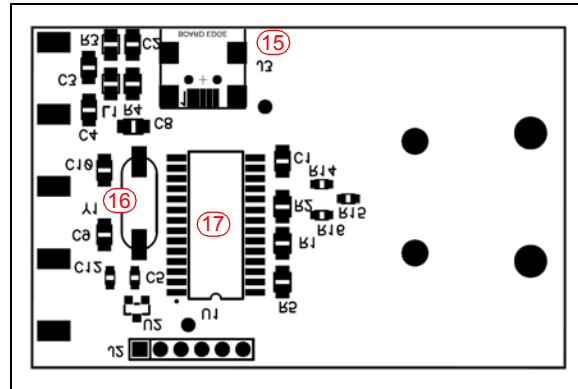


FIGURE 42: 4th Layer – Bottom Silk.

15. The USB connector and its components are isolated from the rest of the circuit.
16. The crystal (XTAL) oscillator is as far from everything else as possible, except from the clock input pins of the microcontroller.
17. The microcontroller produces both thermal and electrical crosstalk, so it is isolated from the analog components.

Figure 43 shows the bottom metal layer of the PCB. The digital circuitry is connected to this layer.

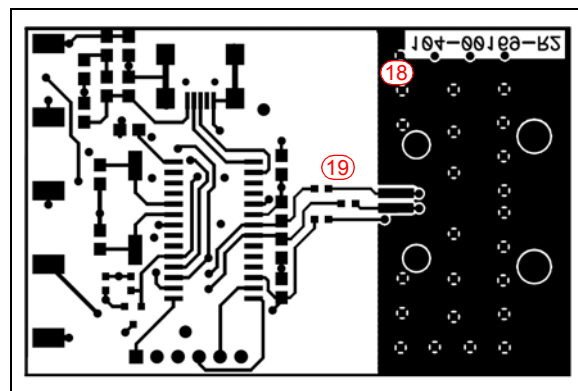


FIGURE 43: 4th Layer – Bottom Metal.

18. Metal fill, connected to the ground plane, minimizes thermal gradients at the cold junction.
19. The digital traces that run under the ground plane extension have series resistors inserted inside the FR4 gap. This reduces the thermal conduction between the sides that solid traces would produce; otherwise this would become the worst case thermal conductor between the microcontroller and the temperature sensors.

SUMMARY

This application note covers thermal effects on Printed Circuit Boards (PCB) encountered in high (DC) precision op amp circuits. Causes, effects and fixes have been covered.

Thermocouple junctions are everywhere on a PCB. The Seebeck effect tells us that these junctions create a thermoelectric voltage. This was shown to produce a voltage across resistors (and other components) in the presence of a temperature gradient.

Preventing large thermoelectric voltages from occurring is usually the most efficient way to deal with thermocouple junctions. The amount of heat generated on the PCB can be reduced, and the heat flow redirected away from critical circuit areas. It also pays to keep any temperature changes from occurring too quickly.

Any remaining thermoelectric voltage effects need to be reduced. Choosing the metals, in critical areas, to have approximately the same work function will minimize the thermoelectric coefficients of the metal junctions. Critical components can be oriented so that they follow constant temperature contour lines. It is possible to cancel most of the thermoelectric voltage effects at the input of op amps by correctly orienting them. Smaller components, spaced closer together, will also help.

Once a design has been implemented on a PCB, it pays to measure its thermal response. Information on where to focus design effort can greatly speed up the design process. Information has been given on measuring temperature, thermal gradients, package θ_{JA} 's and troubleshooting tips and tricks.

Leakage current effects also need to be minimized. Methods to accomplish this for surface and bulk leakage currents have been shown.

Other effects were also discussed.

A design example using the MCP6V01 Thermocouple Auto-zeroed Reference Design PCB illustrates the theory and recommendations given in this application note. The circuit operation is described, then the PCB layout choices are covered in detail.

At the end of this application note, references to the literature and an appendix with the design example's schematic are provided.

REFERENCES

Related Application Notes

- [1] AN990, "Analog Sensor Conditioning Circuits – An Overview," Kumen Blake; Microchip Technology Inc., DS00990, 2005.
- [2] AN1177, "Op Amp Precision Design: DC Errors," Kumen Blake; Microchip Technology Inc., DS01177, 2008.
- [3] AN1228, "Op Amp Precision Design: Random Noise," Kumen Blake; Microchip Technology Inc., DS01228, 2008.

Other Application Notes

- [4] AN990, "Analog Sensor Conditioning Circuits – An Overview," Kumen Blake; Microchip Technology Inc., 2005.
- [5] AN684, "Single Supply Temperature Sensing with Thermocouples," Bonnie C. Baker; Microchip Technology Inc., DS00684, 1998.
- [6] AN679, "Temperature Sensing Technologies," Bonnie Baker, Microchip Technology Inc., DS00679, 1998.

Other References

- [7] User's Guide, "MCP6V01 Thermocouple Auto-Zeroed Reference Design," Microchip Technology Inc., DS51738, 2008.
- [8] "The OMEGA[®] Made in the USA Handbook[™]," Vol. 1, OMEGA Engineering, Inc., 2002.

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APPENDIX A: PCB SCHEMATIC (MCP6V01 THERMOCOUPLE AUTO-ZEROED REFERENCE DESIGN)

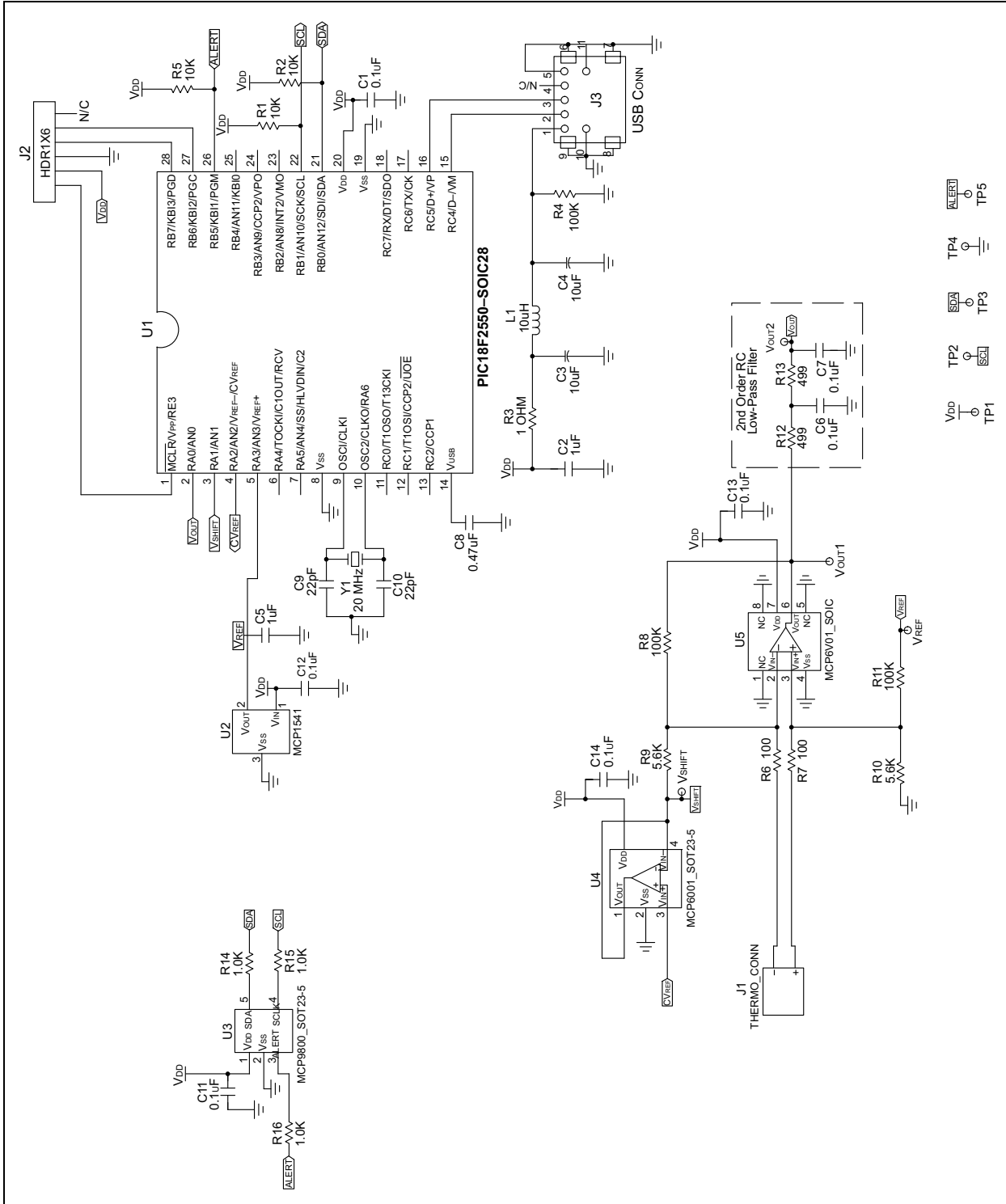


FIGURE A-1: THERMOCOUPLE CIRCUIT'S SCHEMATIC.

APPENDIX B: PCB PARASITIC RESISTANCE

The body of this application note emphasized better PCB designs. For this reason, detailed analyses of leakage currents were not included.

This appendix shows you how to estimate parasitic resistances on a PCB. This will help adjust designs sensitive to leakage currents.

B.1 PCB Resistivities

Surface resistivity (ρ_S , in units of $M\Omega$, or equivalent) describes the local, physical behavior of a PCB surface under a voltage gradient field. The aggregate behavior over all such points creates an equivalent, parasitic surface resistance (R_{PS}) between any two points.

Bulk resistivity (ρ_V , in units of $M\Omega$ cm, or equivalent) describes the local, physical behavior inside a PCB's dielectric under a voltage gradient field. The aggregate behavior over all such points creates an equivalent, parasitic bulk resistance (R_{PB}) between any two points.

Typical resistivities for FR4, based on several manufacturer's data, are:

- $\rho_S \approx 1 \times 10^5 M\Omega$
- $\rho_V \approx 1 \times 10^6 M\Omega$ cm

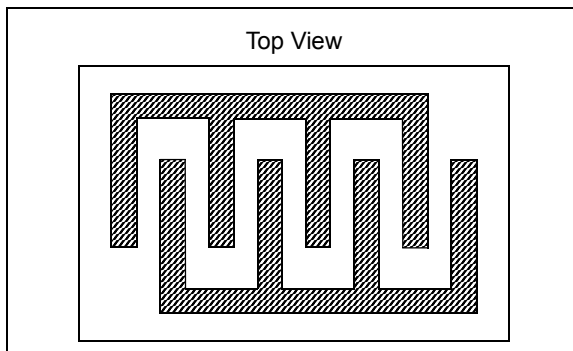
Different operating conditions and manufacturing flows will produce different values; sometimes by two or three orders of magnitude in either direction.

B.2 Measuring Resistivities

Example B-1 shows two parallel, serpentine traces on the same PCB surface. This geometry is useful for measuring ρ_S on a given PCB process. Make the traces as long as possible, and as close together as possible, to maximize the surface leakage current.

For example, a 6 in \times 6 in PCB (60 mil thick) could have two serpentine traces 10 mil wide and 10 mil apart. If the overlap area is 5 in \times 5 in, the equivalent length would be 1250 in. With $\rho_S = 1 \times 10^5 M\Omega$ and $\rho_V \approx 1 \times 10^6 M\Omega$ cm, we estimate $R_{PS} \approx 0.8 M\Omega$ and $R_{PB} \approx 2 G\Omega$.

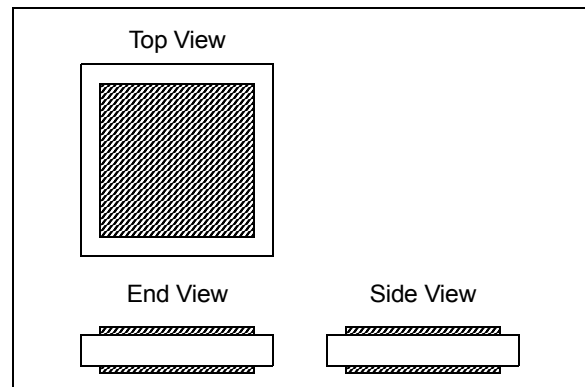
EXAMPLE B-1: PARALLEL TRACES



Example B-2 shows two parallel planes on opposite PCB surfaces. This geometry is useful for measuring ρ_V on a given PCB process. Make the planes as large as possible, to maximize the bulk leakage current.

For instance, a 6 in \times 6 in PCB (60 mil thick) could have two planes 5 in long and 5 in wide. With $\rho_S = 1 \times 10^5 M\Omega$ and $\rho_V = 1 \times 10^6 M\Omega$ cm, we can estimate $R_{PS} \approx \infty$ and $R_{PB} \approx 0.9 G\Omega$.

EXAMPLE B-2: PARALLEL PLANES



Be sure to measure ρ_S and ρ_V under various conditions seen by your circuit. These values will also change between different manufacturers and processes.

B.3 Numerical Solutions

B.3.1 COMMERCIAL SOFTWARE

When optimizing a complicated PCB geometry, it may pay to use a PDE (partial differential equation) solver. Searching the internet for "partial differential equation software," or the equivalent, should bring up several commercially available software packages.

B.3.2 USING SPICE

It is possible to use SPICE to implement a network of resistors representing heat flow between adjacent points.

Select an array of equally spaced points. Resistors connect adjacent points and represent the local resistance to current flow, in that direction.

To simulate a particular parasitic resistance, force a voltage at its input and measure the current at its output. The voltage-to-current ratio is that resistance.

Figure B-1 shows a typical array point, in a two dimensional (2D) array. The central point is at voltage V_0 . The four adjacent points are connected by the four resistors R_1 , R_2 , R_3 and R_4 .

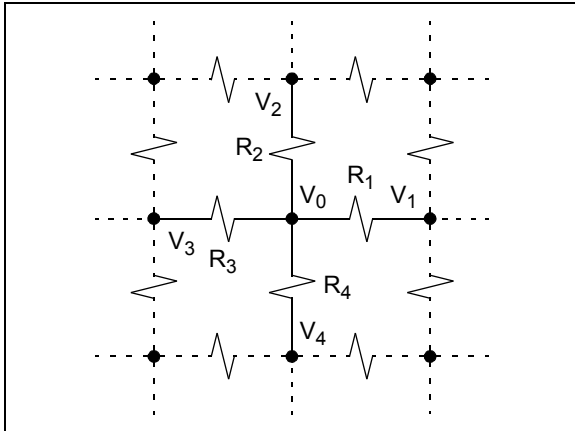


FIGURE B-1: TYPICAL 2D ARRAY.

The resistors represent the local resistivity between adjacent points. Use very low valued resistors for points connected by metal. For instance, R_1 is:

EQUATION B-1:

$$R_1 = \rho_S \Delta x / \Delta y, \text{ for surface calculations}$$

$$= \rho_V \Delta x / (\Delta y \Delta z), \text{ for bulk calculations}$$

Where:

ρ_S = Local Surface Resistivity ($M\Omega$)

ρ_V = Local Bulk Resistivity ($M\Omega \text{ cm}$)

Δx = grid spacing in the x-direction

Δy = grid spacing in the y-direction

Δz = z-dimension (common to all objects)

This approach is easily extended to three dimensions (3D).

B.3.3 USING A SPREADSHEET

It is possible to simulate in a spreadsheet by using an iterative approach. Set up the resistive array like the last section. The iteration equation at V_0 is:

EQUATION B-2:

$$V_0 = (V_1/R_1 + V_2/R_2 + V_3/R_3 + V_4/R_4)$$

$$/ (1/R_1 + 1/R_2 + 1/R_3 + 1/R_4)$$

$$= (V_1 + V_2 + V_3 + V_4) / 4, \text{ all Rs equal}$$

The convergence can be slow, so this approach should be used for simple problems.

Once the voltages are determined, it is a simple matter to calculate the sum of currents into (or out of) a node of interest.

This approach is easily extended to three dimensions (3D).

APPENDIX C: REVISION HISTORY

Revision B (July 2012)

The following is the list of modifications:

1. Added power supply components to circuit diagrams.
2. Re-wrote **Section “Leakage Currents”**, starting on page 11.
 - a) Added information on high impedance sources and parasitic leakage resistances.
 - b) Corrected guard ring connections so they are driven by a low impedance source.
 - c) Added current source examples.
 - d) Added discussion of bulk leakage currents.
 - e) Expanded discussion on isolating sensitive connections from a PCB.
3. Added **Section “Other Tips”**, on page 16.
4. Added AN990 to **Section “References”**, on page 19.
5. Added **Appendix B: “PCB Parasitic Resistance”**, starting on page 21.
6. Added **Appendix C: “Revision History”**, on page 23.

Revision A (March 2009)

- Original Release of this Document.

AN1258

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