

## Power-up Trouble Shooting

*Authors: Mark Pallones,  
Mark Palmer  
Microchip Technology Inc.*

### INTRODUCTION

Application of power to microcontroller devices can cause problems when it is not handled properly. Indication of a problem can range from corrupted memory, to unexpected operation, to no operation at all. Avoiding these problems, the device must go through a certain power-up sequence. The PIC<sup>®</sup> devices integrate several features to simplify the design for the power-up sequence. These integrated features also reduce the total system cost.

This application note describes the requirements for the device to properly power-up, common pitfalls that designers encounter, and methods to assist in solving power-up problems.

### THE POWER-UP SEQUENCE

There are several factors that determine the actual power-up sequence that a device will go through. These factors are:

- The Processor Family
  - PIC16C5X (Baseline)
  - PIC16CXXX (Mid-range)
  - PIC16F1XXX (Enhanced-Mid-range)
  - PIC17CXXX (High-end)
- Oscillator Configuration
- Device Configuration
- MCLR pin

**Note:** The PIC16CXXX family refers to devices with a 14-bit instruction word. This does not include the PIC16C5X family.

The Power-on Reset (POR) signal generation is discussed, followed by the power-up sequence for the specific device families.

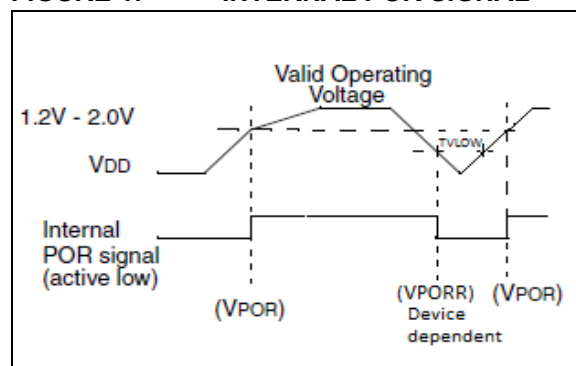
### POWER-ON RESET (POR) SIGNAL

There is a basic requirement to ensure the proper operation of a PIC microcontroller and this is to ensure that device supply voltage VDD is within acceptable operation range before executing the software code. To meet this requirement, a certain sequence of events must happen, and it begins with the Power-on Reset (POR) signal.

The POR signal is a level-triggered signal. Figure 1 shows that when VDD increases from 0V to a level below Power-on Reset Release Voltage (VPOR), the POR signal is active. During this voltage transition, the device is in Reset state. Once VDD crosses the VPOR limit, the POR signal becomes inactive. This event indicates the device has a Power-on Reset (POR) and is already prepared for minimum operation. The VPOR limit is usually determined by a minimum voltage requirement of core logic, RAM data retention, Flash read, Fuse read and internal oscillator. The value of VPOR is somewhere between 1.2-2.0 volts.

VPOR ensures only a minimum operation of the device. It does not ensure that all circuits in the device will function correctly. VDD must reach at least the minimum voltage requirement of device full operation (VDDMIN) before exiting the Reset state.

**FIGURE 1: INTERNAL POR SIGNAL**



When VDD is falling, the voltage at which the POR signal returns active is device-dependent. Some devices have a Power-on Reset Rearm voltage (VPORR) limit. The VPORR can be found in the DC characteristics section of the device data sheet. In [Figure 1](#), when VDD falls below this limit and stays for a duration time of TVLOW, the POR circuit will rearm (accurately monitors the VDD level) and the POR signal becomes active again. When VDD reaches the VPOR limit again, the POR signal becomes inactive and the device leaves the Reset state. However, some of the devices do not have a VPORR limit. To ensure that these devices will have a POR, VDD must return to VSS before power is applied.

The POR signal will be generated regardless of the level of the MCLR pin. The PIC device families vary on what event triggers the next power-up sequence. [Table 1](#) describes the events.

**TABLE 1: EVENTS THAT TRIGGER NEXT POR SEQUENCE**

Device	Events
PIC16C5X	Both the POR signal rising edge and any $\overline{\text{MCLR}}$ rising edge <sup>(1)</sup>
PIC16CXXX	The POR signal rising edge
PIC16F1XXX	The POR signal rising edge
PIC17CXXX	Either the POR signal rising edge or the first $\overline{\text{MCLR}}$ rising edge (if $\overline{\text{MCLR}}$ is low when the POR occurs). After this event, all following $\overline{\text{MCLR}}$ rising edges cause the device to start program execution immediately <sup>(1)</sup> .

**Note 1:** The POR low-to-high transition configures Special Function Register (SFR) bits/registers to a specified value. The SFR bits/registers are not identically affected by the  $\overline{\text{MCLR}}$  signal. Refer to the device data sheet to see how the bits are affected by these two conditions.

The POR sequence for each of the PIC device families is described in the following sections:

- PIC16C5X Family
- PIC16CXXX Family
- PIC16F1XXX Family
- PIC17CXXX Family

## PIC16C5X FAMILY

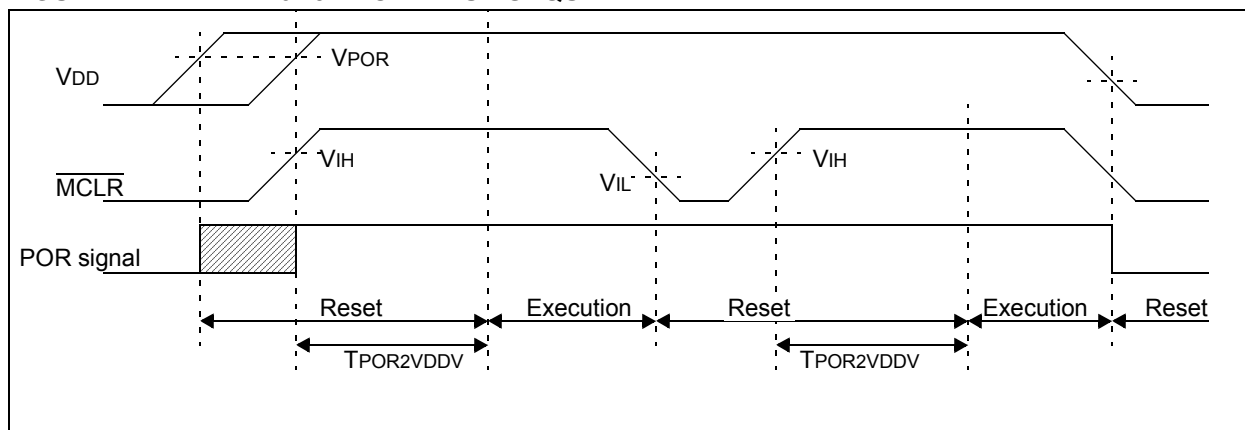
In [Figure 2](#), when the  $\overline{\text{MCLR}}$  pin has reached a high level, the device is held in Reset for the duration of  $\text{TPOR2VDDV}$ .  $\text{TPOR2VDDV}$  is the time provided by the Device Reset Timer (DRT). This time delay allows most crystal (except low-frequency crystals) to start-up and stabilize. DRT used RC oscillator and a 8-bit counter. It provides typically 18 ms time-out on the device at any Oscillator Configuration (see [Table 2](#)). Due to the characteristics of resistor and capacitors, the time-out is extremely variable over temperature and voltage. There could be a device-to-device variation. See the specific device data sheet for the range of this time-out.

**TABLE 2: TIME-OUT IN VARIOUS SITUATIONS (TYPICAL)**

Oscillator Configuration	Power-up	Wake-up from Sleep
XT, HS, LP <sup>(1)</sup>	18 ms	18 ms
RC	18 ms	18 ms

**Note 1:** 32 kHz crystals have a typical start-up time of 1-2 seconds. Crystals >100 kHz have a typical start-up time of 10-20 ms. Resonators are typically <1 ms. All these times are voltage dependent.

**FIGURE 2: PIC16C5X POWER-UP SEQUENCE**



## PIC16CXXX FAMILY

After the POR rising edge has occurred, the device can have up to two time-out sequences that occur in series. The first being the Power-up Timer (PWRT), the second being the Oscillator Start-up Timer (OST).

The Power-up Timer time-out will occur if enable bit PWRTE is read as a '1'. The PWRT uses a 10-bit counter, with the clock from an internal RC. Due to the characteristics of resistors and capacitors, this time is extremely variable over temperature and voltage. There is also a device to device variation. See the data sheet for the range of this time-out.

**Note:** Some devices under mid-range architecture changed the polarity of the PWRTE Configuration bit. Refer to the specific device data sheet for the polarity of this bit.

The OST will occur on power-up/wake-up when the device has Oscillator mode selected. This allows the oscillator to stabilize before program execution begins. The OST uses a 10-bit counter, with the clock from the OSC pin. The time is dependent on the frequency of the input clock. This timer is disabled if the oscillator is configured as RC.

Figure 3 shows how the two timers work in the power-up sequence. VDD must be valid when program execution starts. The  $TPWRT + TOST$  times can be thought of as the time that the device gives for the VDD to become valid ( $TPOR2VDDV$ ). Figure 4 shows when device execution begins for the case of the MCLR pin going high before  $TPOR2VDDV$  times out. Figure 5 shows when the MCLR pin is held low longer than the  $TPOR2VDDV$  time. The device starts execution immediately when MCLR goes high. Table 3 gives typical Reset times.

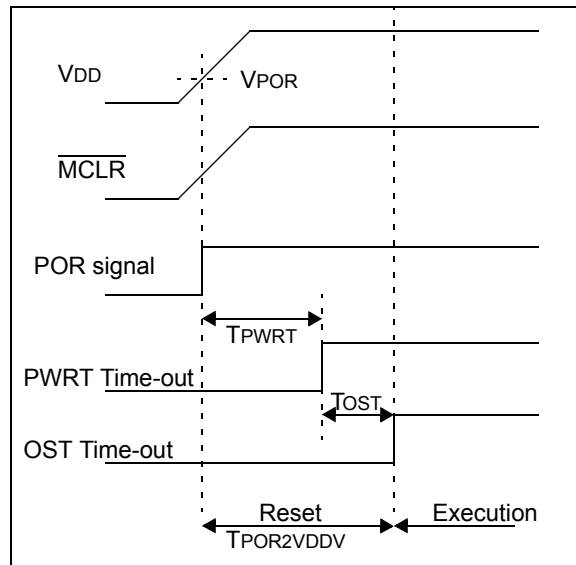
**TABLE 3: TIME-OUT IN VARIOUS SITUATIONS (TYPICAL)**

Oscillator Configuration	Power-up		Wake-up from Sleep
	PWRTE = 1 (2)	PWRTE = 0 (2)	
XT, HS, LP <sup>(1)</sup>	72 ms + 1024 TOSC	1024 TOSC	1024 TOSC
RC	72 ms	—	—

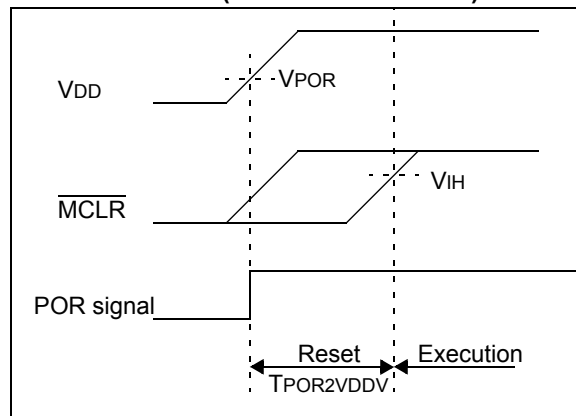
**Note 1:** 32 kHz crystals have a typical start-up time of 1-2 seconds. Crystals >100 kHz have a typical start-up time of 10-20 ms. Resonators are typically <1 ms. All these times are voltage dependent.

**Note 2:** Future devices will change the polarity of this Configuration bit. Refer to the specific data sheet for the polarity of the PWRT Configuration Bit.

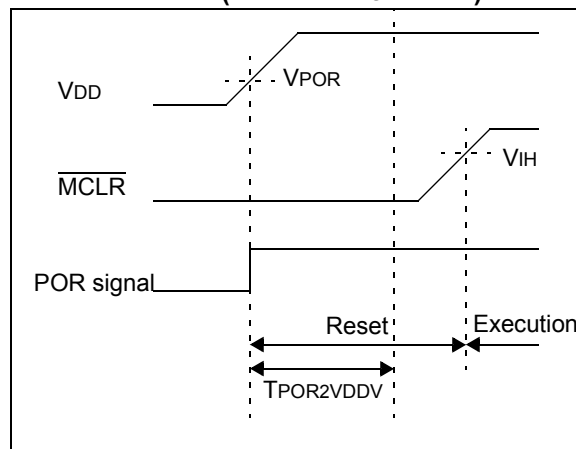
**FIGURE 3: PIC16CXXX POWER-UP SEQUENCE**



**FIGURE 4: START OF DEVICE OPERATION (MCLR < TPOR2VDDV)**



**FIGURE 5: START OF DEVICE OPERATION (MCLR > TPOR2VDDV)**



## PIC16F1XXX FAMILY

Like the PIC16CXXX family, the PIC16F1XXX family has two possible time-outs that can occur in series after the POR signal is asserted. When enabled, Power-up Timer (PWRT) comes first followed by Oscillator Start-up timer (OST). The PWRT, BOR and  $\overline{\text{MCLR}}$  features can be used to extend the start-up period until all device operation conditions have been met.

The PWRT time-out will occur if enable bit  $\overline{\text{PWRTE}}$  is read as a '0' and can be invoked also after Brown-out Reset (BOR). The device is held in Reset as long as PWRT is active. The PWRT delay allows additional time for the VDD to rise an acceptable level. The PWRT uses a 10-bit counter, with the clock from an internal RC. Due to the characteristics of resistors and capacitors, this time is extremely variable over temperature and voltage. There is also a device to device variation. See the data sheet for the range of this time-out.

The OST will occur only for XT, LP and HS mode and only on Power-up, BOR, or wake-up from sleep.

The OST counts the oscillator pulses on the OSC1/CLKIN pin. The counter only starts incrementing after the amplitude of the signal reaches the oscillator

input thresholds. This time-out allows the crystal oscillator or resonator to stabilize before program execution begins. The length of the time-out is a function of the crystal/resonator frequency.

Figures 6 to 9 depict how the two timers work in the power-up sequence.  $\text{TPOR2VDDV}$  denotes the allowable time for the VDD to become valid, which is also equal to the sum of  $\text{TPWRT}$  and  $\text{TOST}$ .  $\text{TOST}$  does not include the time for the crystal/resonator to react to an oscillation level detectable by the OST.

Figure 6 shows when the  $\overline{\text{MCLR}}$  pin is tied to VDD, the code execution starts after  $\text{TPOR2VDDV}$  is over. Figure 7 shows the code execution in the case where the  $\overline{\text{MCLR}}$  pin is released from low before  $\text{TPOR2VDDV}$  times out. Figure 8 shows when the  $\overline{\text{MCLR}}$  pin is held longer than  $\text{TPOR2VDDV}$ . The device executes code immediately when the  $\overline{\text{MCLR}}$  pin goes high. Figure 9 shows the code execution when Two-Speed Start-up mode is enabled. Two-Speed Start-up mode can be enabled through setting the IESO bit in device configuration. This device feature minimizes the latency between external oscillator start-up and code execution. Table 4 gives typical reset time.

FIGURE 6: PIC16F1XXX POWER-UP SEQUENCE ( $\overline{\text{MCLR}}$  TIED TO VDD)

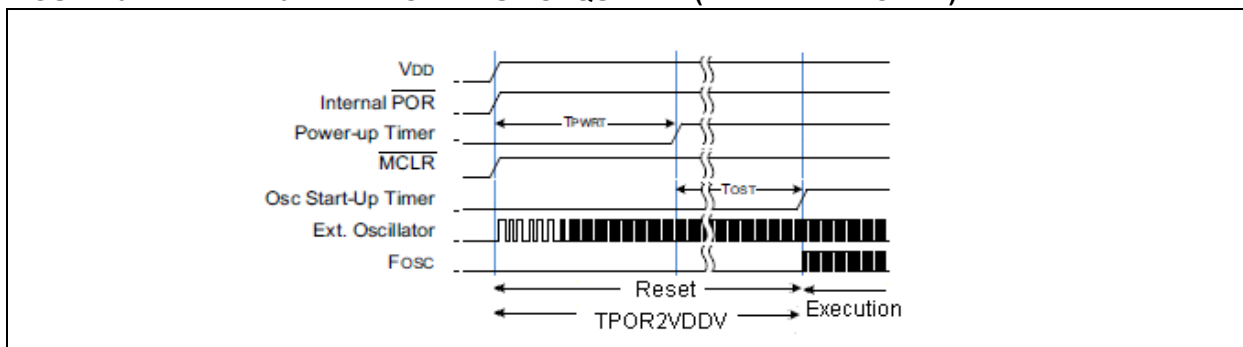
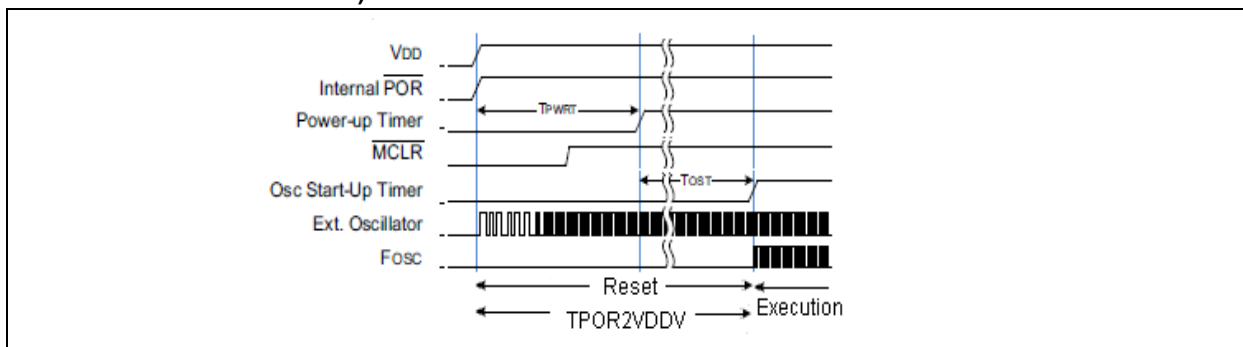
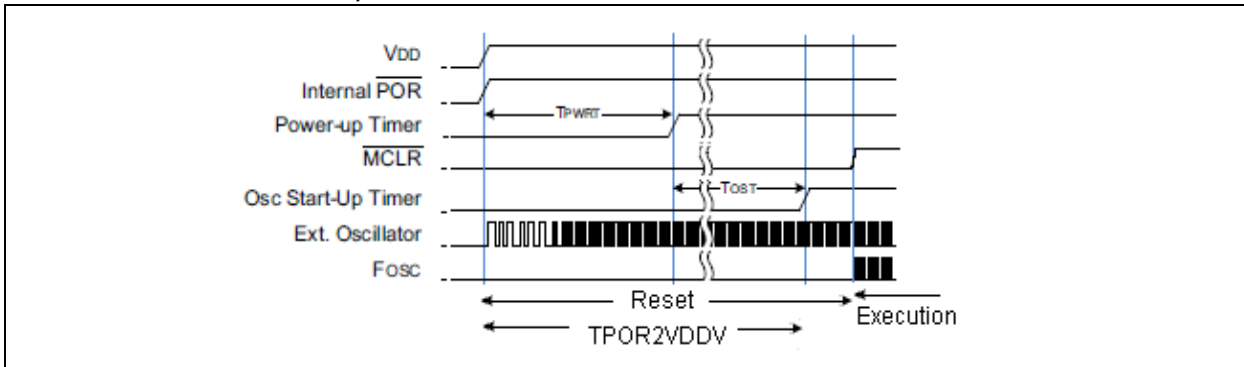


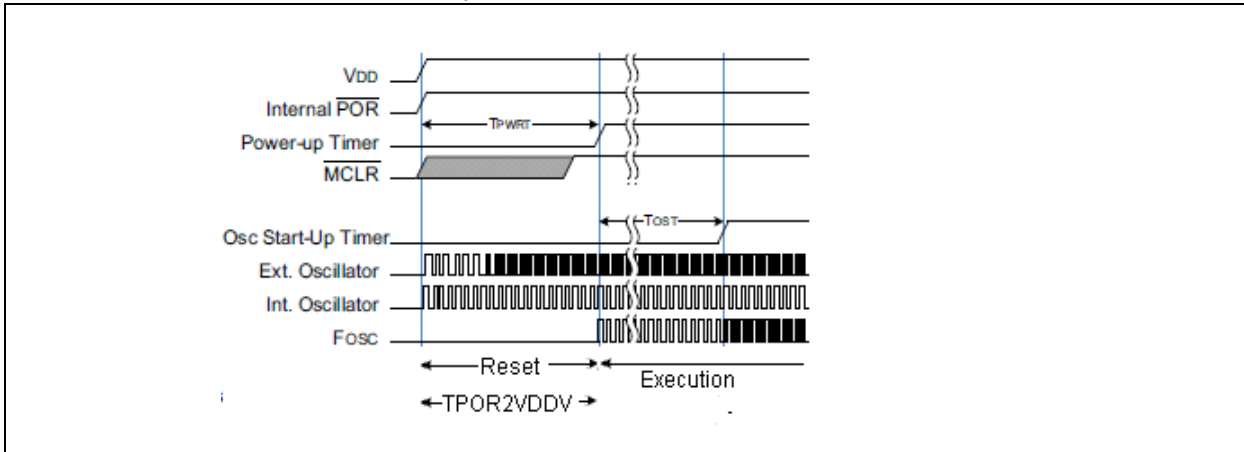
FIGURE 7: PIC16F1XXX POWER-UP SEQUENCE ( $\overline{\text{MCLR}}$  NOT TIED TO VDD AND  $\overline{\text{MCLR}} < \text{TPOR2VDDV}$ )



**FIGURE 8: PIC16F1XXX POWER-UP SEQUENCE ( $\overline{\text{MCLR}}$  NOT TIED TO  $V_{DD}$  AND  $\overline{\text{MCLR}} > \text{TPOR2VDDV}$ )**



**FIGURE 9: PIC16F1XXX POWER-UP SEQUENCE (OSCILLATOR TWO-SPEED START-UP MODE IS ENABLED)**



**TABLE 4: TIME-OUT IN VARIOUS SITUATIONS (TYPICAL)**

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep	
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$
XT, HS, LP <sup>(1)</sup>	65 ms + 1024 $T_{osc}$ <sup>(2)</sup>	1024 $T_{osc}$ <sup>(2)</sup>	65 ms + 1024 $T_{osc}$ <sup>(2)</sup>	1024 $T_{osc}$ <sup>(2)</sup>	1024 $T_{osc}$ <sup>(2)</sup>	1024 $T_{osc}$ <sup>(2)</sup>
RC, EC, INTOSC	65 ms		65 ms			

**Note 1:** 32 kHz crystals have a typical start-up time of 1-2 seconds. Crystals > 100 kHz have a typical start-up time of 10-20 ms. Resonators are typically < 1 ms. All these times are voltage dependent.

**2:** Oscillator Two-Speed Start-up mode is disabled.

## PIC17CXXX FAMILY

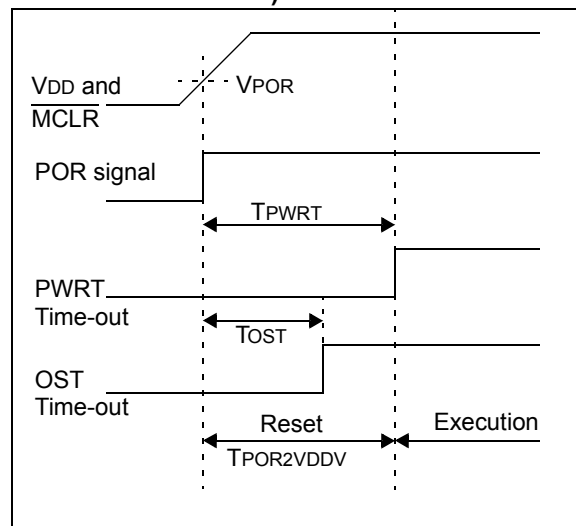
When the  $\overline{\text{MCLR}}$  pin comes to a high level, after the POR rising edge, the device has two time-out sequences that occur in parallel. One is the Power-up Timer (PWRT), the other is the Oscillator Start-up Timer (OST). The timer with the greater time holds the device in Reset. Figure 11 shows the sequence with  $\overline{\text{MCLR}}$  tied to VDD. Figure 12 shows the time-out when  $\overline{\text{MCLR}}$  is independent of VDD. The PWRT time is generally longer, except for low-frequency crystals/resonators. The OST time does not include the start-up time of the oscillator/resonator.

The PWRT uses a 10-bit counter, with the clock from an internal RC. The characteristics of the RC vary from device to device and overtemperature and voltage. The specification for the time-out range can be found in the electrical specification of the data sheet.

The OST uses a 10-bit counter, with the clock from the OSC pin. The time is dependent on the frequency of the input clock.

Until  $\overline{\text{MCLR}}$  has reached a high level, the next POR sequence will not start. While the POR signal remains high, all following  $\overline{\text{MCLR}}$  pulses will not cause the POR sequences to occur (Figure 12).

**FIGURE 10: PIC17CXXX POWER-UP SEQUENCE (MCLR TIED TO VDD)**

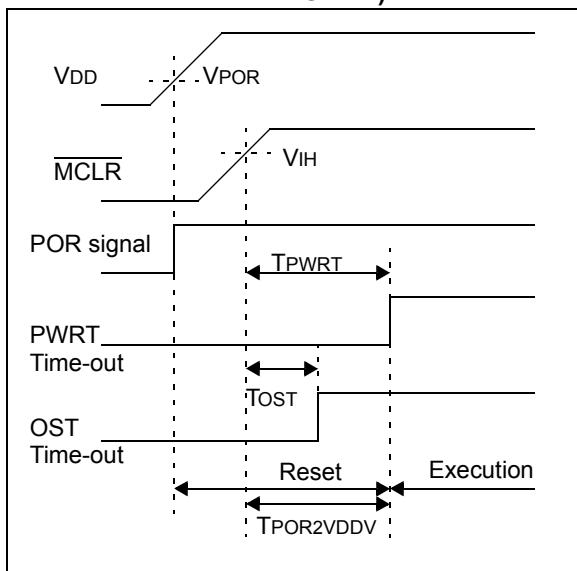


**TABLE 5: TIME-OUT IN VARIOUS SITUATIONS (TYPICAL)**

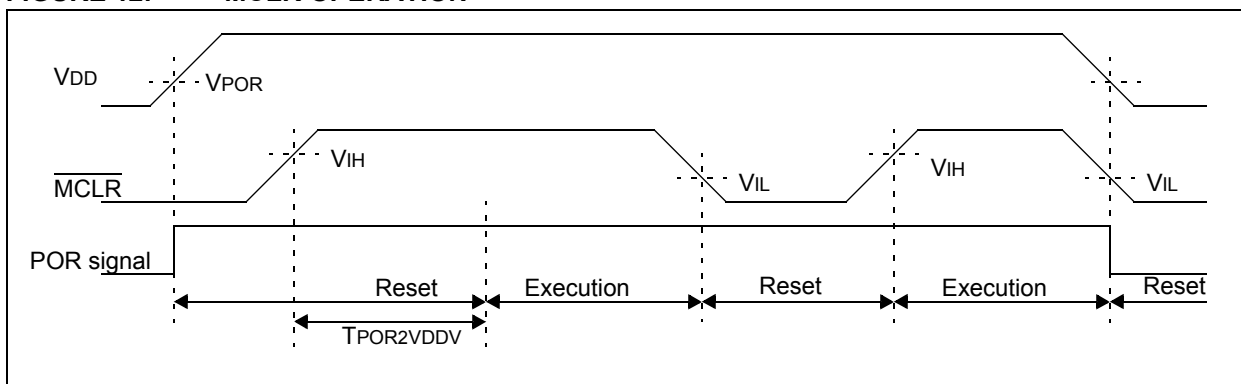
Oscillator Configuration	Power-up	Wake-up from Sleep
RC, EC	Greater of 80 ms and 1024 TOSC	—
XT, LF <sup>(1)</sup>	Greater of 80 ms and 1024 TOSC	1024 TOSC

**Note 1:** 32 kHz crystals have a typical start-up time of 1-2 seconds. Crystals >100 kHz have a typical start-up time of 10-20 ms. Resonators are typically <1 ms. All these times are voltage dependent.

**FIGURE 11: PIC17CXXX ( $\overline{\text{MCLR}}$  NOT TIED TO VDD)**



**FIGURE 12:  $\overline{\text{MCLR}}$  OPERATION**



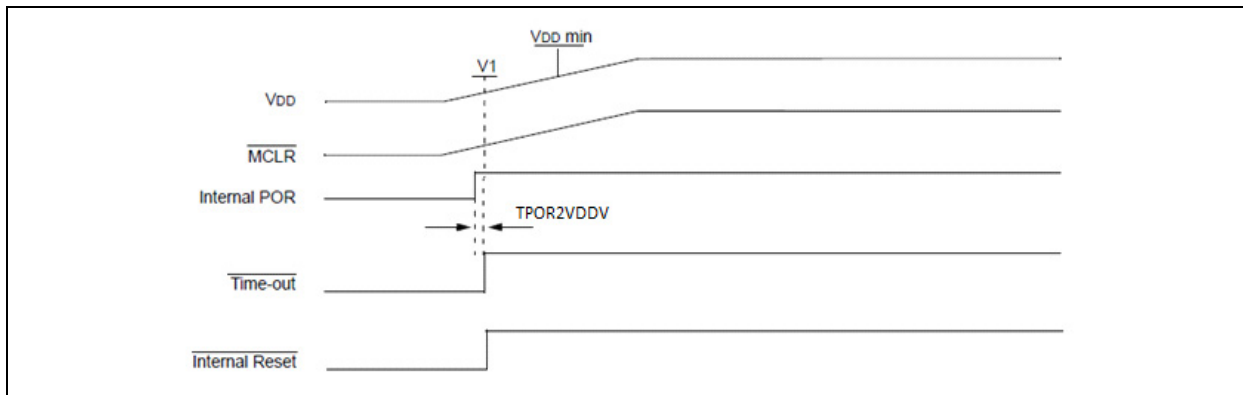


## POWER-UP CONSIDERATIONS

The device must be at a valid operating voltage when the device exits Reset. This can be done by ensuring that the power supply rise time is fast enough to reach an operating level. The rise time must be faster than 0.05 V/ms.

When VDD rise time is very slow, a potential problem might occur. In Figure 13, when VDD reached V1, time-out already expired, internal Reset ended, and the device attempts to execute code. Since V1 is lower than VDDMIN, the device may not function properly.

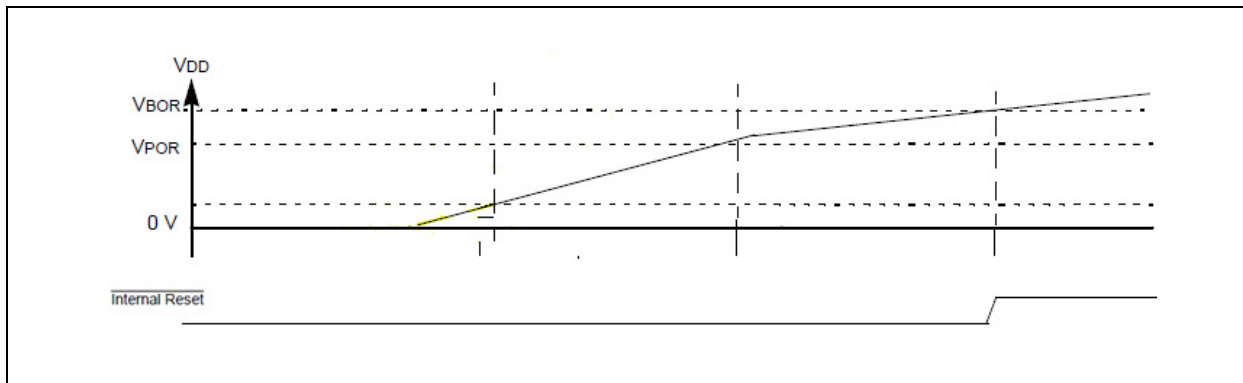
**FIGURE 13: MCLR TIED TO VDD SLOW VDD RISE TIME**



This potential problem can be avoided if the device has an internal BOR circuit. Although the typical function of BOR is to put the device in Reset during a brown-out condition, BOR can also be used to extend device Reset during power-up (See Figure 14). When BOR is enabled, the device will remain in Reset until VDD

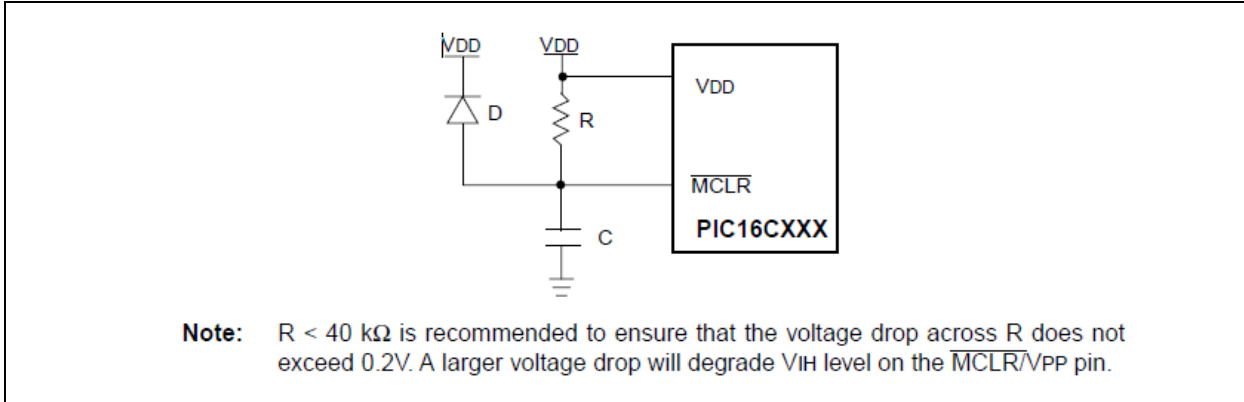
reaches the BOR voltage limits, VBOR. BOR can be enabled through device Configuration Word bit BOREN. On some devices, VBOR is fixed, but on others it can be selected from several different voltages. VBOR limit is usually determined by a minimum VDD required by the device.

**FIGURE 14: RISING VDD WITH BOR EVENT**



In some devices where the POR circuit alone monitors VDD rise, MCLR should be held low until operating VDD level has been reached. This can be done using an external POR circuit (see Figure 15).

**FIGURE 15: EXTERNAL POR CIRCUIT**



When the rise time of VDD is very fast, there will be a time delay before the Power-on Reset (POR) signal will rise to a logic high (TTP2PORH). This delay is in the 1-5 ms range, as shown in Figure 16.

Figure 17, Figure 18, and Figure 19 show the maximum time from the POR sequence beginning to the device having a valid operating voltage. Table 6 gives the TPOR2VDDV times. When determining the time at which VDD must be valid, the VPOR limit must be assumed to be at the minimum VPOR limit.

### How Crystal Frequencies Affect Start-up Time

PIC16CXXX, PIC16F1XXX and PIC17CXXX families may have start-up times that include the contributions of the oscillator. Table 6 shows how the oscillator can affect each mode of operation, with Table 7 giving the Reset time that an oscillator generates. This time can

be used in the equation to calculate the total Reset time, at the given frequency. This time may vary slightly due to the initial start-up characteristics of the crystal/oscillator circuit.

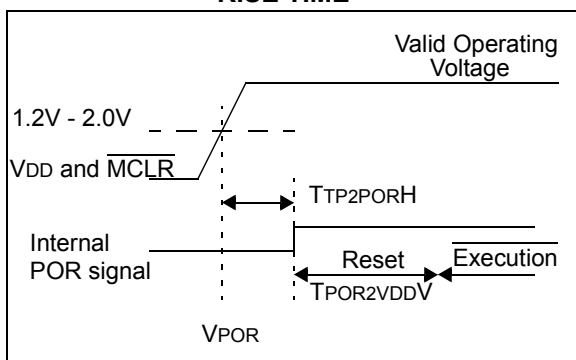
**Note 1:** The rise time specification does not ensure that a valid VDD operating voltage will be reached before the device exits Reset. The device's VDD must be within the specified operating range for proper device operation.

**2:** The start-up characteristics of the crystal/oscillator must also be taken into account when determining the time that the device must be held in Reset.

**TABLE 6: MAXIMUM TIME FROM POR RISING EDGE TO VALID VDD VOLTAGE**

Device Family	OSC Mode	Maximum Time	Condition
PIC16C5X	LP, XT, HS and RC	9 ms	
PIC16CXXX	RC	28 ms	PWRTE = 1
	LP, XT and HS	28 ms + 1024 TOSC	PWRTE = 1
	LP, XT and HS	1024 TOSC	PWRTE = 0
PIC16F1XXX	RC, EC, INTOSC	64 ms	PWRTE = 0
	LP, XT and HS	64 ms + 1024 TOSC	PWRTE = 0, IESO = 0
	LP, XT and HS	1024 TOSC	PWRTE = 1, IESO = 0
PIC17CXXX	LP, XT, EC and RC	Greater of (40 ms or 1024 TOSC)	

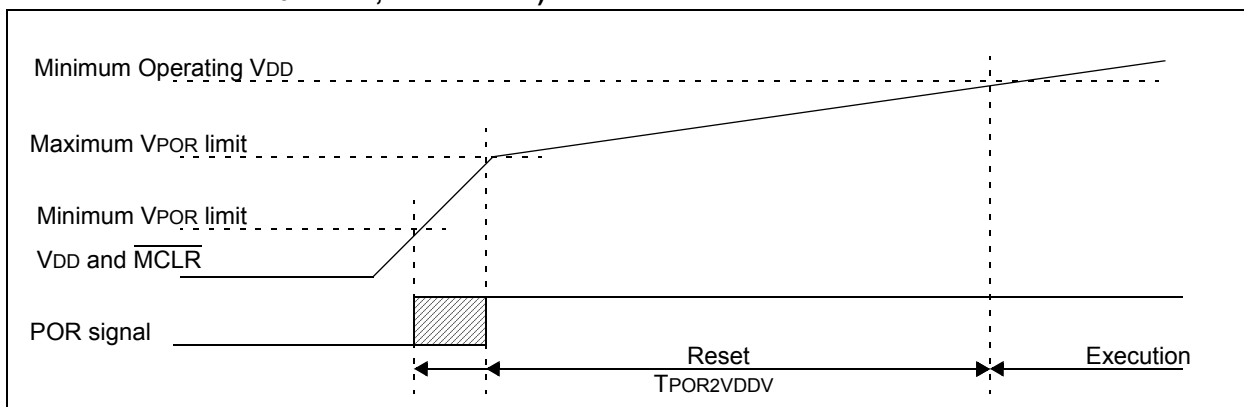
**FIGURE 16: POR DELAY FOR FAST V<sub>DD</sub> RISE TIME**



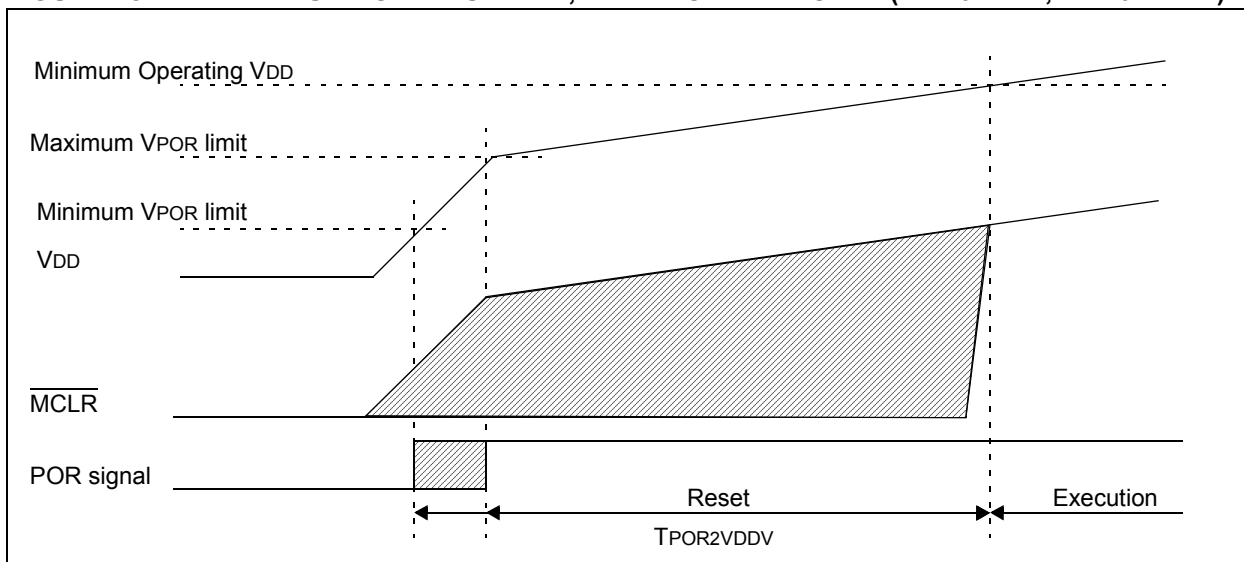
**TABLE 7: RESET TIME DUE TO OSCILLATOR**

	Clock Frequency								
	32 kHz	1 MHz	2 MHz	4 MHz	8 MHz	10 MHz	16 MHz	20 MHz	25 MHz
1024 TOSC	32 ms	1.0 ms	512 ms	256 ms	128 ms	102.4 ms	64 ms	51.2 ms	41 ms

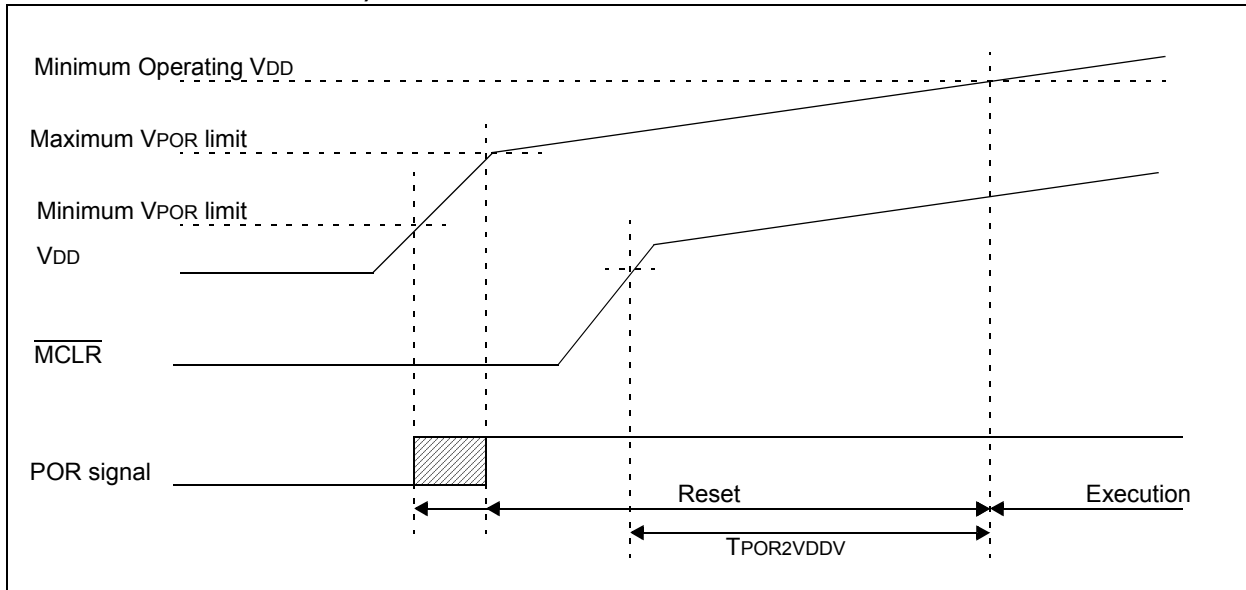
**FIGURE 17: MAXIMUM POWER-UP TIME,  $\overline{\text{MCLR}}$  TIED TO V<sub>DD</sub> (PIC16C5X, PIC16CXXX, PIC16F1XXX, PIC17CXXX)**



**FIGURE 18: MAXIMUM POWER-UP TIME,  $\overline{\text{MCLR}}$  NOT TIED TO V<sub>DD</sub> (PIC16CXXX, PIC16F1XXX)**



**FIGURE 19: MAXIMUM POWER-UP TIME,  $\overline{\text{MCLR}}$  NOT TIED TO  $V_{\text{DD}}$  (PIC16C5X AND PIC17CXXX)**



## OSCILLATOR AND RESONATOR CONSIDERATIONS

Oscillators and resonators from different manufacturers may have different characteristics. The recommended capacitor selection can be found in each device's data sheet. When we do the capacitor selection, during the oscillator/resonator characterization, we are currently using devices from one of several manufacturers. Generally, we use oscillators from either ECS, CTS, FOX or Epson, and ceramic resonators from either Murata Erie or Panasonic. Other manufacturers may be used in the future, depending on availability and other factors.

Other manufacturers devices may have significantly different characteristics. To ensure proper oscillator operation, the circuit should be verified at the lowest temperature/highest VDD (to ensure that the crystal is not overdriven), and with the highest temperature/lowest VDD (to ensure the device still starts up) that the device will be subjected to while in the application. This ensures a stable start-up and frequency for this device, at the extreme conditions of the application.

For production purposes, the above testing should be done with many different samples of the components selected. This is so the part to part variation of the capacitors, resistors, crystals/resonators, and PIC devices are taken into account. All PIC device final data sheets supply the characterization information on the transconductance of the oscillator (measurement of gain). This information can be used to check part to part variations of the PIC device.

When selecting the crystal, the designer must ensure that it is a parallel cut type. Failure to use a parallel cut crystal may cause:

- Frequency operation out of the specified range of the crystal.
- Unreliable oscillator start-up.
- Device or crystal damage.

## RAM AND SPECIAL FUNCTION REGISTER INITIALIZATION

After a successful Power-up Reset, the device will begin to execute the firmware program. To have expected operation, ALL RAM should be initialized by the program. This includes the Special Function Registers (SFR) and the general purpose data memory. The use (read) of an uninitialized RAM location will cause the program to do exactly what you told it, with the unexpected RAM value. It should not be expected that all devices will power-up with the same uninitialized device values.

There are many factors that contribute to how a RAM cell powers up, but the most common pitfall is between the Windowed and OTP device types. Many times, a user forgets to cover the window after erasing the Windowed device. When the device is powering up, and the light is able to shine onto the device die, the transistor characteristics will shift. This can cause the device RAM to have a different power-up value than a device where no light can shine onto the die (OTP or covered).

**Note:** RAM locations should be initialized before they are used. Use of an uninitialized location will cause proper device operation with the improper values. That is, it will do what you told it to do, not what you wanted it to do.

## VALID OPERATING VOLTAGE LEVELS

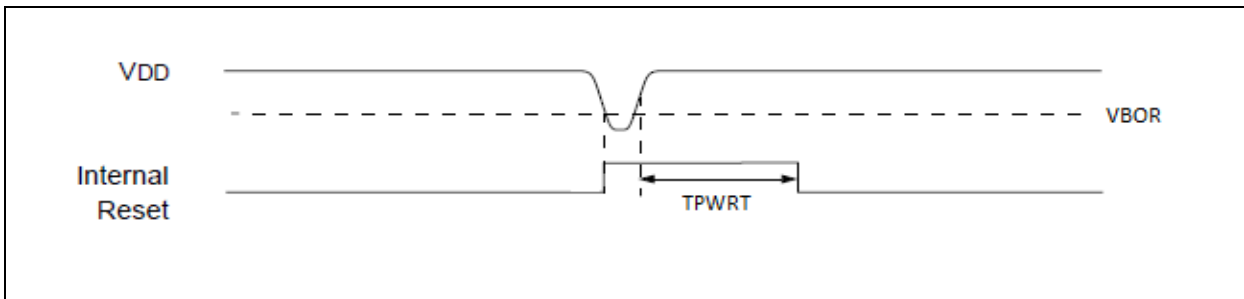
When the device is operating, the device voltage must be within the specified Min/Max limits. Operation of the device outside these limits may cause unexpected device operation.

One of the primary functional failure modes of a device is when the applied voltage is lower than the specified minimum requirement. This functional failure is called Brown-out. Brown-out causes the program memory not to be read correctly. For example, the program counter may be pointing to a `MOVE` instruction, but the device reads it as a `GOTO` instruction (with a random

destination). This can have disastrous effects to the operation of the application. If brown-out conditions are possible, the application needs to be protected by using a brown-out circuit.

Some PIC devices have an on-chip BOR circuit. As mentioned earlier, this feature is intended primarily to put the device in Reset when brown-out condition occurs. When BOR is enabled and VDD falls below VBOR for a duration of TBOR, the device will hold in Reset. The device will remain in Reset until VDD rises again above VBOR. However, when PWRT is enabled, the device will remain in Reset for additional time specified by TPWRT. (see [Figure 20](#)).

**FIGURE 20: BROWN-OUT SITUATION**



When the devices do not have an on-chip BOR circuit or the application requires a different level of detection than the BOR trip point, an external BOR circuit may be implemented. [Figure 21](#), [Figure 22](#) and [Figure 23](#) show

examples of external BOR circuit. Each needs to be evaluated to determine if they match the requirements of the application.

**FIGURE 21: EXTERNAL BROWN-OUT CIRCUIT 1**

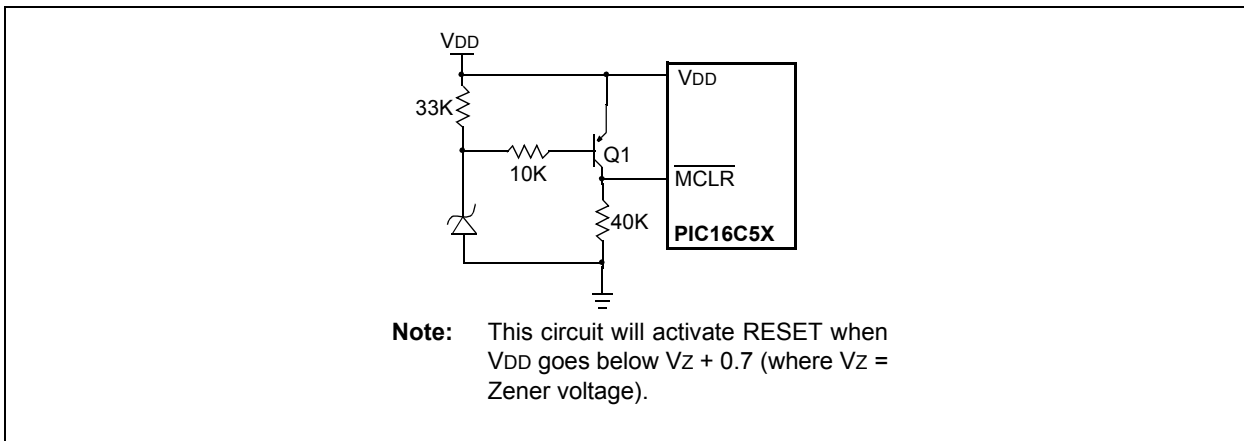


FIGURE 22: EXTERNAL BROWN-OUT CIRCUIT 2

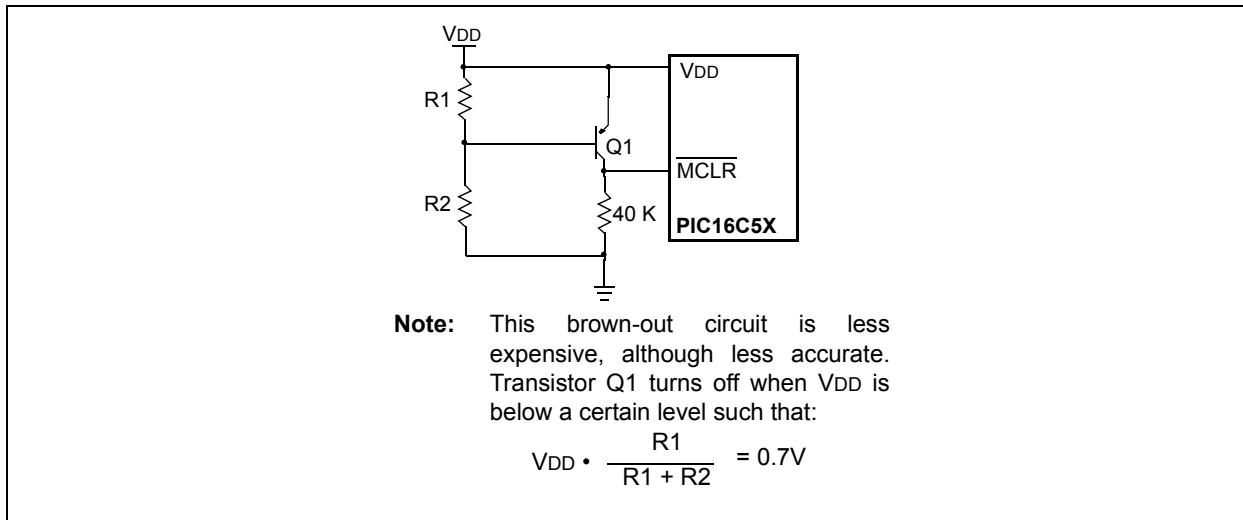
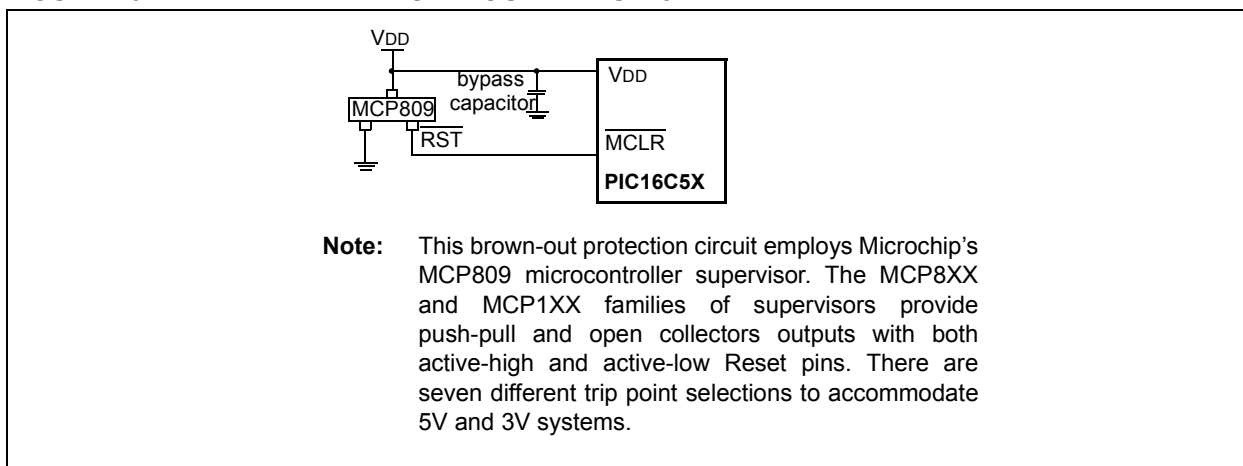


FIGURE 23: EXTERNAL BROWN-OUT CIRCUIT 3



## BROWN-OUT AND THE WDT

The recommended solution for brown-out conditions is to enable the BOR feature, if available in the device, or use an external brown-out circuit. This will keep the device in Reset until a valid operating voltage is present. In the case where the device does not have a BOR feature, the additional cost of the external brown circuit can be traded off with system recovery from brown-out. Using a Watchdog Timer (WDT) can enhance the probability of system recovery from a brown-out condition.

**Note:** If I/O drive conflicts can cause critical problems, this technique should not be used. This is due to the indeterminate time before a device Reset could occur, which would reset all pins to inputs to eliminate any I/O conflict.

When using the WDT in brown-out conditions, care must be taken. Brown-outs may cause an unrecoverable condition, but with good design practice the probability of this can be significantly reduced.

During a brown-out, improper program execution can occur due to an EPROM read failure. This program execution can also corrupt data memory locations, which include the Special Function Registers (SFRs). Corrupting the control registers may cause hardware conflicts. For example, an input may become an output. Other conflicts are possible, but the situation will be application dependent.

As the device voltage gets lower, internal logic can become corrupted. This can include the Program Counter (PC) value, Stack Pointer and contents, state machines, data memory, etc.

When a valid voltage is returned, the device may be at an unexpected program location, possibly using corrupted values. In this situation, the device would not be expected to operate as intended and could get into a state that appears locked-up.

For the PIC17C42 in Code-Protected Microcontroller mode, once the Program Counter (PC) exceeds the 32K word boundary, the device will become locked-up. The PC can exceed the 32K word boundary from the execution of incorrect instructions (due to failure reading the EPROM) or by the PC becoming corrupted.

If the WDT is to be used to reset the device, care must be used in structuring the program. Optimally, only one CLRWDT instruction should be used. This minimizes the possibility of program execution returning to a loop which clears the WDT. This loop could then lock-up the device, since other control registers are corrupted and the device is not configured as expected. An example is; if the loop was waiting for an interrupt, but the bit that enables global interrupts was disabled, the device would no longer respond to the interrupts and would appear locked-up.

**Example 1** shows a simple implementation of using the WDT Reset for system recovery. The program loops, waiting for a WDT Time-out (which clears the  $\overline{TO}$  bit). After the WDT Reset, the  $\overline{TO}$  bit needs to be set (by executing a CLRWDT instruction). The program should then initialize the device. Then application code can start executing. There is a possibility of the  $\overline{TO}$  bit being corrupted by low voltage, and the device not being in a Reset state when the software initializes the device.

The WDT example in **Appendix B: “Test Programs”** uses a different method, independent of the  $\overline{TO}$  bit. This uses RAM locations which get loaded with a value. A WDT Time-out (or other Reset) needs to occur. The RAM locations are verified to contain the same values. Once the RAM is verified, it is cleared, and the device should be initialized. These RAM locations can be used by the application program.

### EXAMPLE 1: USING WDT RESET

```
org    Reset_Address
      GOTO    TO_TEST    ;At any reset,
                        ;test the  $\overline{TO}$  bit

org    TO_TEST
      BTFSC  STATUS, TO ;WDT Time-Out?
HERE   GOTO  HERE      ;NO, Wait for  $\overline{TO}$ 
Time_Out
      CLRWDT           ;YES, Good Reset
      :               ;Start here
      :               ;Initialize
Device :               ;Application Code
```

## FALSE POWER-DOWN

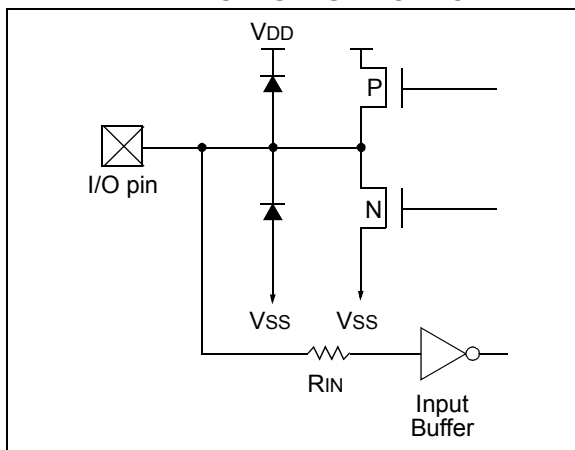
In applications where power is removed from the device's supply lines, but voltage is still applied to an I/O pin, unexpected operation may occur. Power is able to be supplied to the device through this I/O pin. Since the device is still partially powered, the internal logic is never completely powered down. **Figure 24** shows the general structure of an I/O pin. **Figure 25** depicts the internal voltage level that is actually applied to some device logic, versus what is seen at the pin.

To ensure a Power-on Reset (POR) rising edge, the device voltage (VDD) must start from Vss. When the device is inadvertently powered from an I/O pin, the voltage at the VDD pin may appear to be near ground but may actually be higher in the device. With some of the internal logic powered, the characteristics of the device can be similar to a brown-out situation. Similar design practices to brown-out should be implemented.

A method for protecting the device from being powered from an I/O pin is shown in **Figure 26**.

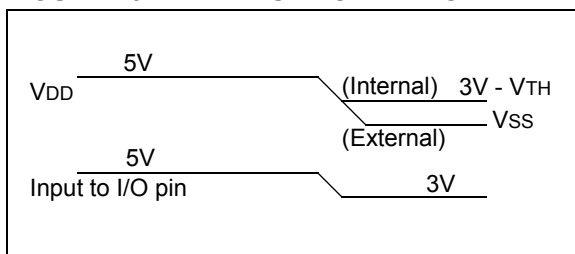


**FIGURE 24: TYPICAL ELECTRICAL STRUCTURE OF I/O PIN**

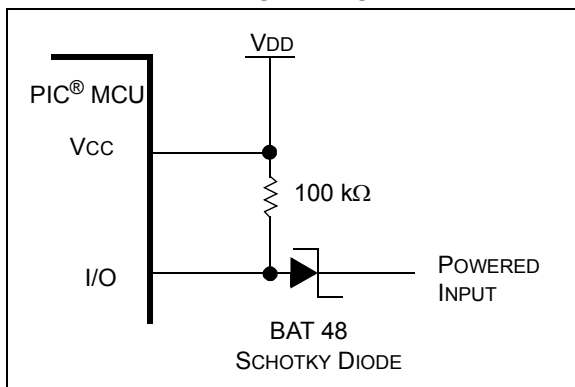


Another case of false power-down situations is when the power is removed from the system, but the capacitor loading keeps a non-zero voltage on the VDD pin. When power is reapplied, the device never powered down so no Power-on-Reset will occur. Enable BOR feature if available in the device or a simple brown-out circuit should fix this.

**FIGURE 25: FALSE POWER-DOWN**



**FIGURE 26: POWERED -INPUT PROTECTION**



In general, an on-chip or external brown-out circuit should cause the PIC device to reset. This ensures that the internal logic is in a known state until a valid device voltage level is reached. The brown-out detection depends on the voltage range of the device and the application requirements. A comprehensive brown-out detection would use a dedicated device to monitor the voltage and force the MCLR pin low, when the voltage becomes lower than specified.

## TROUBLESHOOTING

There are several techniques that can be used to troubleshoot problems related to powering up. First it is important to try to locate the source of the problem.

These sources could be:

- No oscillation on OSC1/OSC2 pins
- Improper/no Program Execution

In cases where there is no oscillation on the OSC1/OSC2 pins, some of the following should be tried:

1. Verify that there are good connections/the components are good.
2. Verify that the crystal/resonator manufacturer is one that has been tested. If not, try other capacitor values.
3. See if an external clock (from a function generator) causes device operation to begin.
4. Verify that all components are well-grounded.
5. If a scope probe is connected to the oscillator output, it must be a low-capacitance/high-impedance probe. If it is not, the oscillator may stop.

In cases where program execution is not as expected:

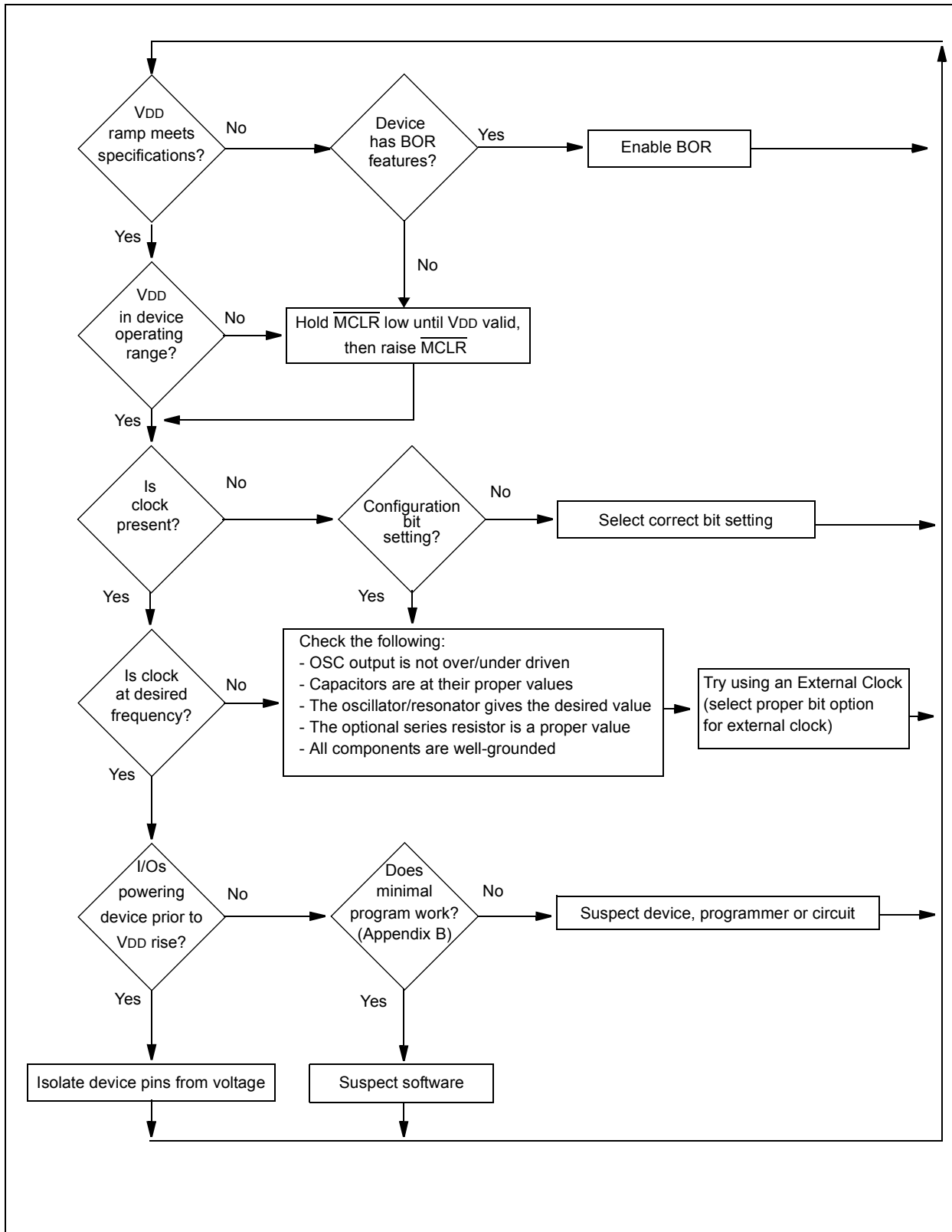
1. Use a minimal program with external clock input.
2. Tie MCLR to ground until solid power is applied to the device then release MCLR (bring high).
3. Measure VDD rise time, if slower than the minimum rise time requirement, determine if the device has a feature to extend the reset time during power-up and enable it. If not available, use external reset circuit.
4. Verify that the device program memory and Configuration bits are programmed to their expected states.

The flowchart shown in [Figure 27](#) can be used to troubleshoot power-up problems. This flowchart is only intended to be the first level diagnostic in trying to solve a power-up problem. Many other flowcharts can be used, depending on the characteristics of the problem and the set-up of the application.

## CONCLUSION

Understanding the criteria for the powering up of a device will allow you to make better design choices. If device power-up problems are still encountered, many techniques can be used to solve the problem. [Appendix B: "Test Programs"](#) contains example code which can be used to verify that a device is operating (powered-up correctly). This eliminates the possibility of the program as the cause, and allows debug on the hardware.

FIGURE 27: TROUBLESHOOTING FLOWCHART



## APPENDIX A: Q & As

Q. **When I use a windowed device (JW), my application works as expected. When I program an OTP device, it no longer works as expected. Why is this?**

A. The silicon is the same between the OTP and windowed devices. If the windowed device's window is not covered (with black tape), light shines onto the silicon. The light causes the potential levels of gates to shift. This in turn can cause RAM to be initialized to an unknown state, which could be different than in the OTP device. If RAM is not initialized by the program before it is used, these different power-up states of the RAM could be the cause of the problem. Ensure that all RAM is initialized in the device. This includes the SFRs.

Q. **My oscillator is not oscillating, what could be wrong?**

A. There are several possibilities, some which include:

1. The wrong oscillator bit setting is selected. The erased (default) state is RC Oscillator mode.
2. The wrong capacitor values are installed. Refer to the most current data sheet for recommended values.
3. The characteristics of your manufacturers crystal are different than those that are characterized by Microchip. Generally, our tests have been done with one of the following manufacturers' crystals/resonators: ECS, FOX, Murata Erie, or Panasonic.
4. The external connections to the device are wrong. Verify that all connections to the device are correct and that good signals/levels are being applied.
5. The cut of the crystal is a series type, as opposed to the specified parallel type.
6. No bypassing capacitors were used on the device. The noise on VDD could be affecting the oscillator circuitry.

Q. **The device was powered-down and then powered back up, but the device does not operate. What could be wrong.**

A. Possibilities include:

1. If power was applied to an I/O pin when the device was "powered-down", the device would be powered through the I/O pin. The internal logic is not actually powered-down, and Power-on Reset (POR) will not occur.
2. When VDD was powered-down, VDD was not given enough time to settle to 0V.
3. The VDD ramp rate is too slow.

Q. **My oscillator is oscillating, but the device is not working. What could be wrong?**

A. There are several possibilities, some which include:

1. Slow VDD rise time, which was too slow to cause a Power-on Reset (POR). The rise time should not exceed the minimum device specification. For most devices this is 0.05 V/ms. Also the device must be at the minimum operating VDD of the processor when Reset is exited.
2. Ensure that the  $\overline{\text{MCLR}}$  pin is not low. This holds the device in Reset.
3. A brown-out has occurred, and has corrupted the internal state machines (including the WDT). Enable the BOR feature if available in the device or an external brown-out circuit recommended to hold the device in Reset during the brown-out condition.
4. The  $\text{CLRWDT}$  instruction is not being used (often enough) when the WDT is enabled.

Q. **When I power-up the device, it does not operate and it gets hot.**

A. Your design is probably permitting fast high voltage signals (spike) onto one of the device pins. This sudden high voltage (and associated current) is in excess of the protection diode limit. The device must be powered-down (to VSS) to release this condition. This condition may cause a functional failure or affect device reliability. All Microchip devices meet or exceed the Human Body Model (HBM) and Machine Model (MM) for ESD and latch-up.

Q. ***My oscillator is oscillating, but not at the expected frequency. What could be wrong?***

A. For many designers, working with oscillators and their related issues can be complicated, since the characteristics can vary widely between manufacturers. Microchip has application notes on oscillators available at [www.microchip.com](http://www.microchip.com). Some quick possibilities are:

1. The cut of the crystal is a series type, as opposed to the specified parallel type.
2. No bypassing capacitors were used on the device. The noise on VDD could affect the oscillator circuitry.
3. The capacitor values used are causing the oscillator to operate in one of the harmonic frequencies.

**Note:** This is not an all inclusive list. You may need to investigate other design aspects.

Q. ***The device seems to never exit Reset, or is continually resetting.***

A. The CLRWDT instruction is not being used (often enough) when the WDT is enabled.

Q. ***The device was powered-down and back up again, but it does not reset. It just starts operating immediately.***

A. Possibilities include:

1. If power was applied to an I/O pin when the device was "powered-down", the device would be powered through the I/O pin. The internal logic is not actually powered-down, and a Power-on Reset (POR) will not occur.
2. When VDD was powered down, VDD was not given enough time to settle to 0V.

Q. ***The oscillator is operating (I check it with a scope), yet when I look at other pins the program is not executing. Why?***

A. One possible reason is that when the oscilloscope probe is placed on the OSC2 pin, the additional capacitance is enough to cause oscillation to start. Removing the capacitive load of the probe causes the oscillation to stop.

## APPENDIX B: TEST PROGRAMS

**Software License Agreement**

The software supplied herewith by Microchip Technology Incorporated (the "Company") is intended and supplied to you, the Company's customer, for use solely and exclusively with products manufactured by the Company.

The software is owned by the Company and/or its supplier, and is protected under applicable copyright laws. All rights are reserved. Any use in violation of the foregoing restrictions may subject the user to criminal sanctions under applicable laws, as well as to civil liability for the breach of the terms and conditions of this license.

THIS SOFTWARE IS PROVIDED IN AN "AS IS" CONDITION. NO WARRANTIES, WHETHER EXPRESS, IMPLIED OR STATUTORY, INCLUDING, BUT NOT LIMITED TO, IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE APPLY TO THIS SOFTWARE. THE COMPANY SHALL NOT, IN ANY CIRCUMSTANCES, BE LIABLE FOR SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, FOR ANY REASON WHATSOEVER.

**EXAMPLE B-1: PIC16C5X BIT TOGGLE**

```

MPASM 01.02.04 Intermediate   C5X_B0T.ASM   12-20-1994   9:25:7                PAGE 1

LOC OBJECT CODE      LINE SOURCE TEXT
VALUE

0001          LIST    P = 16C54,  F = INHX8M, n = 66
0002 ;
0003 ;*****
0004 ;
0005 ; This program is a minimum program to toggle a single I/O port pin for the
0006 ; 16C5x family of devices. The only initialization is that of the data
0007 ; direction register (TRIS) of the I/O pin and the Toggling of the pin.
0008 ; The waveform will be 1 unit high and 3 units low.
0009 ;
0010 ;      Program:      C5X_B0T.ASM
0011 ;      Revision Date: 12-20-94
0012 ;
0013 ;*****
0014 ;
0015 ;
0016 ; HARDWARE SETUP
0017 ;      None
0018 ;
0019 ;
0020          INCLUDE <p16C5x.inc>
0021 ;
0022 ; P16C5X.INC Standard Header File, Version 0.1      Microchip Technology, Inc.
0023 ;
0024 ;
0025 ;
0026 ;*****
0027 ;
0028 START
0029          CLRF    STATUS          ; POWER_ON Reset (Beginning of program)
0030          MOVLW  0x00             ; Do initialization (Bank 0)
0031          MOVWF  PORTB           ; Specify value for PortB output latch
0032          MOVLW  0x00             ; Specify which PortB pins are inputs / outputs
0033          TRIS   PORTB           ;
0034 ;
0035 lzz      BSF    PORTB, 0        ; B0 is High
0036          BCF    PORTB, 0        ; B0 is Low
0037          GOTO   lzz             ; Loop
0038 ;
0039 ;
0040 ;
0041 ;
0042 ; Reset address. Determine type of RESET
0043 ;
0044          IFDEF  __16C54

```

**EXAMPLE B-2: PIC16C5X BIT TOGGLE**

```

01FF          0045 RESET_V    EQU    0x1FF
              0046     ENDIF
              0047 ;
              0048     IFDEF    __16C54A
              0049 RESET_V    EQU    0x1FF
              0050     ENDIF

              0051 ;
              0052     IFDEF    __16C55
              0053 RESET_V    EQU    0x1FF
              0054     ENDIF
              0055 ;
              0056     IFDEF    __16C56
              0057 RESET_V    EQU    0x3FF
              0058     ENDIF
              0059 ;
              0060     IFDEF    __16C57
              0061 RESET_V    EQU    0x7FF
              0062     ENDIF
              0063 ;
              0064     IFDEF    __16C58A
              0065 RESET_V    EQU    0x7FF
              0066     ENDIF
              0067 ;
01FE          0068 PROG_MEM_END EQU    RESET_V - 1
              0069 ;
              0070 ;
              0071     org     PROG_MEM_END        ; End of Program Memory
01FE 0BFE     0072 ERR_LP_1    GOTO    ERR_LP_1      ; If you get here your program was lost
              0073 ;
              0074     org     RESET_V            ; RESET vector location
01FF 0A00     0075 R_VECTOR    GOTO    START        ;
              0076 ;
              0077 ;
              0078     end
              0079
              0080
              0081

```

MEMORY USAGE MAP ('X' = Used, '-' = Unused)

```

0000 : XXXXXXXX-----
0040 : -----
0180 : -----
01C0 : -----XX

```

All other memory blocks unused.

```

Errors   :    0
Warnings :    0
Messages :    0

```

## EXAMPLE B-3: PIC16CXXX BIT TOGGLE

```

MPASM 01.02.04 Intermediate  CXX_B0T.ASM  12-20-1994  10:18:22                PAGE  1

LOC  OBJECT CODE      LINE SOURCE TEXT
VALUE

0001          LIST    P = 16C74,  F = INHX8M,  n = 66
0002 ;
0003 ;*****
0004 ;
0005 ; This program is a minimum program to toggle a single I/O port pin for the
0006 ; 16Cxx family of devices. The only initialization is that of the data
0007 ; direction register (TRIS) of the I/O pin and the Toggling of the pin.
0008 ; The waveform will be 1 unit high and 3 units low.
0009 ;
0010 ;           Program:           CXX_B0T.ASM
0011 ;           Revision Date:     12-20-94
0012 ;
0013 ;*****
0014 ;
0015 ;
0016 ; HARDWARE SETUP
0017 ;           None
0018 ;
0019 ;
0020           INCLUDE <p16Cxx.inc>
0021 ;
0022 ; P16CXX.INC Standard Header File, Version 0.2      Microchip Technology, Inc.
0023 ;
0024 ;*****
0025 ;*****      Start program here.
0026 ;*****
0027 ;
0000          0028 START
0000 0183      0029          CLRF   STATUS           ; POWER_ON Reset (Beginning of program)
0001 3000      0030          MOVLW 0x00           ; Do initialization (Bank 0)
0002 0086      0031          MOVWF PORTB          ; Specify value for PortB output latch
0003 1683      0032          BSF    STATUS, RP0       ; Bank 1
0004 3000      0033          MOVLW 0x00           ; Specify which PortB pins are inputs / outputs
0005 0086      0034          MOVWF TRISB          ;
0006 1283      0035          BCF    STATUS, RP0       ; Bank 0
0007          0036 ;
0007 1406      0037 lzz          BSF    PORTB, 0       ; B0 is High
0008 1006      0038          BCF    PORTB, 0       ; B0 is Low
0009 2807      0039          GOTO   lzz           ; Loop
0010          0040 ;
0011          0041 ;
0012          0042 ;
0013          0043 ;
0014          0044 ; End of Program Memory
0015          0045 ;
0016          0046          IFDEF __16C71
0017          0047 PROG_MEM_END EQU    0x3FF
0018          0048          ENDIF
0019          0049 ;
0020          0050          IFDEF __16C71A
0021          0051 PROG_MEM_END EQU    0x3FF
0022          0052          ENDIF
0023          0053 ;
0024          0054          IFDEF __16C73
0025          0055 PROG_MEM_END EQU    0xFFF
0026          0056          ENDIF
0027          0057 ;
0028          0058          IFDEF __16C74
0029          0059 PROG_MEM_END EQU    0xFFF
0030          0060          ENDIF
0031          0061 ;
0032          0062          IFDEF __16C61
0033          0063 PROG_MEM_END EQU    0x3FF
0034          0064          ENDIF
0035          0065 ;
0036          0066          IFDEF __16C63

```



**EXAMPLE B-4: PIC16CXXX BIT TOGGLE**

```

0067 PROG_MEM_END EQU 0x7FF
0068 ENDIF
0069 ;
0070 IFDEF __16C64
0071 PROG_MEM_END EQU
0x7FF
0072 ENDIF
0073 ;
0074 IFDEF __16C65
0075 PROG_MEM_END EQU 0xFFF
0076 ENDIF
0077 ;
0078 IFDEF __16C84
0079 PROG_MEM_END EQU 0x3FF
0080 ENDIF
0081 ;
0082 IFDEF __16C84A
0083 PROG_MEM_END EQU 0x3FF
0084 ENDIF
0085 ;
0086 ;
0087 org PROG_MEM_END ; End of Program Memory
0088 ERR_LP_1 GOTO ERR_LP_1 ; If you get here your program was lost
0089 ;
0090 ;
0091 end
0092
0093
0094
0095

MEMORY USAGE MAP ('X' = Used, '-' = Unused)

0000 : XXXXXXXXXXXX-----
0040 : -----

0F80 : -----
0FC0 : -----X

All other memory blocks unused.

Errors : 0
Warnings : 0
Messages : 0

```

**Note:** Special Function Register data memory locations, in Bank 1, are specified by their true address in the file PIC16CXXX.INC. The use of the MPASM™ assembler will generate a warning message, when those labels are used with direct addressing. Warning messages can be turned off with an assembler option.

**EXAMPLE B-5: PIC16F1XXX BIT TOGGLE**

```
File Name: PIC16F1XX toggle bit.asm
;
;
;Summary:
;This program is a minimum program to toggle a single I/O port pin for the
;16F1XXX family devices.
;
;
;
;Generation Information:
;      Device      : PIC16F1xxx
;      Compiler    : MPASMWIN v5.54
;      MPLAB       : MPLAB X IDE v2.0
;*****
;
;*****
;Copyright (c) 2013 released Microchip Technology Inc. All rights reserved.
;
;Microchip licenses to you the right to use, modify, copy and distribute
;Software only when embedded on a Microchip microcontroller or digital signal
;controller that is integrated into your product or third party product
;(pursuant to the sublicense terms in the accompanying license agreement).
;
;You should refer to the license agreement accompanying this Software for
;additional information regarding your rights and obligations.
;
;SOFTWARE AND DOCUMENTATION ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND,
;EITHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY WARRANTY OF
;MERCHANTABILITY, TITLE, NON-INFRINGEMENT AND FITNESS FOR A PARTICULAR PURPOSE.
;IN NO EVENT SHALL MICROCHIP OR ITS LICENSORS BE LIABLE OR OBLIGATED UNDER
;CONTRACT, NEGLIGENCE, STRICT LIABILITY, CONTRIBUTION, BREACH OF WARRANTY, OR
;OTHER LEGAL EQUITABLE THEORY ANY DIRECT OR INDIRECT DAMAGES OR EXPENSES
;INCLUDING BUT NOT LIMITED TO ANY INCIDENTAL, SPECIAL, INDIRECT, PUNITIVE OR
;CONSEQUENTIAL DAMAGES, LOST PROFITS OR LOST DATA, COST OF PROCUREMENT OF
;SUBSTITUTE GOODS, TECHNOLOGY, SERVICES, OR ANY CLAIMS BY THIRD PARTIES
;(INCLUDING BUT NOT LIMITED TO ANY DEFENSE THEREOF), OR OTHER SIMILAR COSTS.
;*****

#include <p16F1XXX.inc>

;This configuration bits setting may change from device to device

__CONFIG __CONFIG1, _FOSC_XT & _WDTE_OFF & _PWRTE_OFF & _MCLRE_OFF & _CP_OFF & _CPD_OFF & _BOREN_ON &
_CLKOUTEN_OFF & _IESO_OFF & _FCMEN_OFF
```

**EXAMPLE B-6: PIC16F1XXX BIT TOGGLE**

```
__CONFIG __CONFIG2, _WRT_OFF & _VCPEN_OFF & _PLLEN_OFF & _STVREN_OFF & _BORV_HI & _LVP_OFF

    org 0x00
    goto START

    org 0x04
    retfie

    org 0x05
START
    banksel PCON          ;goto BANK1
MMP    btfsc  PCON,NOT_POR ;check if POR occurs
        goto  MMP        ;if not code will stay in the MMP loop

MCG    btfsc  PCON,NOT_BOR ;check if BOR occurs
        goto  MCG        ;if not code will stay in the MCG loop

    banksel TRISB        ;goto BANK1
    movlw  0x00          ;initialize PortB pins as an outputs
    movwf  TRISB
    banksel PORTB        ;goto BANK0
    movlw  0x00          ;initialize PORTB
    movwf  PORTB

    banksel PORTB        ;if POR and BOR occur RB1 toggles
MUP    bsf    PORTB, RB1  ;RB1 is high
        bcf    PORTB, RB1 ;RB1 is low
        goto  MUP        ;MUP loop

    END
```

## EXAMPLE B-7: PIC17CXXX BIT TOGGLE

```

MPASM 01.02.04 Intermediate P17_B0T.ASM 12-19-1994 17:15:3 PAGE 1

LOC OBJECT CODE      LINE SOURCE TEXT
VALUE

0001          LIST    P = 17C42, F = INHX32, n = 66
0002 ;
0003 ;*****
0004 ;
0005 ; This program is a minimum program to toggle a single I/O port pin for the
0006 ; 17Cxx family of devices. The only initialization is that of the data
0007 ; direction register (DDR) of the I/O pin and the Toggling of the pin.
0008 ; The waveform will be 1 unit high and 1 unit low.
0009 ;
0010 ;      Program:      P17_B0T.ASM
0011 ;      Revision Date: 12-20-94
0012 ;
0013 ;*****
0014 ;
0015 ;
0016 ; HARDWARE SETUP
0017 ;      None
0018 ;
0019 ;
0020          INCLUDE <p17Cxx.inc>
0021 ;
0022 ; P17CXX.INC Standard Header File, Version 0.2      Microchip Technology, Inc.
0023 ;
0024 ;
0025 ;
0026 ;*****
0027 ;
0028 START
0029          CLRF    ALUSTA      ; POWER_ON Reset (Beginning of program)
0030          CLRF    BSR        ; Do initialization
0031          MOVLW  0x00        ; Bank 0
0032          MOVWF  PORTB       ; Specify value for PortB output latch
0033          MOVLW  0x00        ;
0034          MOVWF  DDRB       ; Specify which PortB pins are inputs / outputs
0035 ;
0036 lzz      BTG     PORTB, 0   ; Toggle level on B0
0037          GOTO   lzz        ; Loop
0038 ;
0039 ;
0040 ;
0041 ;
0042 ; End of Program Memory
0043 ;
0044          IFDEF  _17C42
0045          PROG_MEM_END EQU 0x7FF
0046          ENDIF
0047 ;
0048 ;
0049          org    PROG_MEM_END ; End of Program Memory
0050 ERR_LP_1  GOTO   ERR_LP_1   ; If you get here your program was lost
0051 ;
0052 ;
0053          end
0054
0055

MEMORY USAGE MAP ('X' = Used, '-' = Unused)

0000 : XXXXXXXX-----
0040 : -----

0780 : -----
07C0 : -----X

All other memory blocks unused.

Errors      : 0
Warnings    : 0
Messages    : 0

```

**EXAMPLE B-8: WDT RESET WITH RAM VERIFY**

```

MPASM 01.20 Released          BO_RAMT.ASM   6-30-1995  16:04:36          PAGE 1

LOC OBJECT CODE      LINE SOURCE TEXT
VALUE
00001          LIST    P = 17C44,  F = INHX32,  n = 66
00002 ;
00003 ;*****
00004 ;
00005 ; This program is a minimum program to recover from a brown-out condition thru
00006 ; the use of the WDT. The method is to load RAM locations with a known value
00007 ; and compare these locations after any RESET. If the RAM location matches the
00008 ; expected value then program flow can continue. The longer this RAM string
00009 ; is, the greater the probability that the RAM would NOT power up in that state.
00010 ;
00011 ;
00012 ; NOTE: This does not Guarantee device recovery, due to the random start-up
00013 ; point after brown-out. This point could be a loop with a CLRWDT
00014 ; instruction. The recommended solution is to always use a brown-out
00015 ; circuit.
00016 ;
00017 ; Program:          B0_RAMT.ASM
00018 ; Revision Date:   06-29-95
00019 ;
00020 ;*****
00021 ;
00022 ;
00023 ; HARDWARE SETUP
00024 ; None
00025 ;
00026 ;
0001 00027 TRUE      EQU    1
0000 00028 FALSE     EQU    0
00029 ;
0001 00030 Debug      EQU    TRUE
00031 #define      __CONFIG__ FUSES
00032 ;
00033          INCLUDE <DEV_FAM.inc>
00102 list
00034 ;
00035 if ( P16C5X )
00036     INCLUDE <p16C5x.inc>
00037     __CONFIG ( _CP_OFF & _WDT_ON & _XT_OSC )
00038 endif
00039 ;
00040 if ( P16CXX )
00041     INCLUDE <p16Cxx.inc>
00042     __CONFIG ( _CP_OFF & _WDT_ON & _XT_OSC & _PWRTE_ON )
00043 endif
00044 ;
00045 if ( P17CXX )
00046     INCLUDE <p17Cxx.inc>
00001 LIST
00002 ; P17CXX.INC Standard Header File, Version 2.01      Microchip Technology, Inc.
00298 LIST
FE00 FFE2 00047     __CONFIG ( _MC_MODE & _WDT_NORM & _XT_OSC )
00048 endif
00049 ;
00050 if ( P16C5X + P16CXX + P17CXX != 1 )
00051 MESSG "WARNING - USER DEFINED: One and only one device family can be selected"
00052 endif
00053 ;
00054          INCLUDE <BO_RAMT.inc>
00029 list
00055          INCLUDE <PMEM_END.inc>
00116 list
00056 ;
00057 ;
00058 ;*****
00059 ;****          Start program here.
00060 ;*****
00061 ;
0000 00062 org Reset_Address
00063 ;          ; in the LIST directive

```

## EXAMPLE B-9: WDT RESET WITH RAM VERIFY

```

00064     if ( P16C5X )
00065     org 0h                ; Override the start of this code.
00066         CLRF STATUS      ; Force program memory to Page 0
00067         CLRF FSR          ; Force Data Memory to Bank 0
00068     endif
00069 ;
00070     if ( P16CXX )
00071         CLRF PCLATH       ; Force program memory to Page 0
00072         CLRF STATUS      ; Force Data Memory to Bank 0
00073     endif
00074 ;
00075     if ( P17CXX )
00076         CLRF PCLATH, F    ; Force program memory to Page 0
0000 2903 00077         CLRF BSR, F    ; Force Peripheral / GP Data Memory to Bank 0
0001 290F 00078     endif
00079 ;
0002 C100 00080         GOTO RAM_TEST    ; At any reset,
00081         ; test the RAM
00082 ;
00083 ; In RAM_TEST, program execution is held-off until a valid "warm" reset
00084 ; occurs. That is, the contents of some RAM locations retain the
00085 ; values that were written to them. The probability that the RAM would power-up
00086 ; in that state is dependent on the number of bytes of RAM used. The
00087 ; more RAM, the less the probability (probability = 1 / ( 2 ** 8(N+1) ).
00088 ;
00089 ;
0100     00090     org MAIN                ; In Program Memory Page 0
0100     00091 RAM_TEST
0100 B0A5 00092         MOVLW BYTE_0
0101 0520 00093         SUBWF RAM0, F
0102 9204 00094         BTFSS STATUS, Z    ; Result = 0?
0103 C110 00095         GOTO LD_RAM      ; NO, Load Ram
00096 ;
0104 B00F 00097         MOVLW BYTE_1    ; YES, Check next
0105 0521 00098         SUBWF RAM1, F    ; location
0106 9204 00099         BTFSS STATUS, Z    ; Result = 0?
0107 C110 00100         GOTO LD_RAM      ; NO, Load RAM
00101 ;
00102 ;         ; YES, Do Again
00103 ;
00104 ;
0108 B05A 00105         MOVLW BYTE_n    ; YES, Check nth
0109 0522 00106         SUBWF RAMn, F    ; location
010A 9204 00107         BTFSS STATUS, Z    ; Result = 0?
010B C110 00108         GOTO LD_RAM      ; NO, Load RAM
00109 ;
00110     if ( P16C5X || P16CXX )
00111         CLRF RAM0        ; YES, Time-out
00112         CLRF RAM1        ; occurred, clear
00113 ;         ; RAM locations
00114 ;
00115         CLRF RAMn        ;
00116     endif
00117 ;
00118 ;
00119     if ( P17CXX )
010C 2920 00120         CLRF RAM0, F    ; YES, Time-out
010D 2921 00121         CLRF RAM1, F    ; occurred, clear
00122 ;         ; RAM locations
00123 ;
010E 2922 00124         CLRF RAMn, F    ;
00125     endif
00126 ;
010F C117 00127         GOTO Time_Out    ; Initialize Device
00128
0110     00129 LD_RAM
0110 B0A5 00130         MOVLW BYTE_0    ; Load RAM
0111 0120 00131         MOVWF RAM0      ; locations to
0112 B00F 00132         MOVLW BYTE_1    ; compare against

```

**EXAMPLE B-10: WDT RESET WITH RAM VERIFY**

```

0113 0121      00133      MOVWF  RAM1      ;
                00134 ;      :
0114 B05A      00135      MOVLW  BYTE_n     ;
0115 0122      00136      MOVWF  RAMn      ;
                00137 ;
0116 C116      00138 HERE   GOTO   HERE      ; Wait for WDT TO
0117           00139 Time_Out ; YES, Good Reset
0117 0004      00140      CLRWDT      ; Start here
                00141 ;      :
                00142 ;      :
                00143 ;      :
                00144 ;      :
                00145      if ( Debug )      ;
                00146      if ( P16C5X )      ;
                00147          CLRF  PORTB      ; PORTB output latch is cleared
                00148          MOVLW  0x00      ;
                00149          TRIS  PORTB      ; Port B is output
                00150          BCF  PORTB, 0 ;
                00151          BSF  PORTB, 0 ; Toggle pin B0
                00152      endif
                00153      if ( P16CXX )      ;
                00154          CLRF  PORTB      ; PORTB output latch is cleared
                00155          BSF  STATUS, RP0      ; Bank 1
                00156          CLRF  TRISB      ; Port B is output
                00157          BCF  STATUS, RP0      ; Bank 0
                00158          BCF  PORTB, 0 ;
                00159          BSF  PORTB, 0 ; Toggle pin B0
                00160      endif
                00161 ;
                00162      if ( P17CXX )      ;
0118 2912      00163          CLRF  PORTB, F      ; PORTB output latch is cleared
0119 2911      00164          CLRF  DDRB, F      ; Port B is output
011A 8812      00165          BCF  PORTB, 0 ;
011B 8012      00166          BSF  PORTB, 0 ; Toggle pin B0
                00167      endif
                00168      endif
                00169 ;
011C C117      00170      GOTO   Time_Out      ; Return to start of Program
                00171 ;
1FFF           00172      org    PROG_MEM_END      ; End of Program Memory
1FFF           00173 ERR_LP_1
1FFF DFFF      00174      GOTO   ERR_LP_1      ; If you get here your program was lost
                00175 ;
                00176      if ( P16C5X )      ;
                00177          NOP      ; This will cause the Program memory rollover
                00178          ; for PIC16C5x devices
                00179      endif
                00180 ;
                00181 ;
                00182      end

```

MEMORY USAGE MAP ('X' = Used, '-' = Unused)

```

0000 : XXX-----
0040 : -----
0100 : XXXXXXXXXXXXXXXXXXXX XXXXXXXXXXXXXXXX-----
0140 : -----
1F80 : -----
1FC0 : -----X
FE00 : X-----
FE40 : -----

```

All other memory blocks unused.

```

Errors      : 0
Warnings    : 0
Messages    : 0

```

---

---

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### **Trademarks**

The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC<sup>32</sup> logo, rPIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MTP, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.


Analog-for-the-Digital Age, Application Maestro, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniclient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rLAB, Select Mode, SQI, Serial Quad I/O, Total Endurance, TSHARC, UniWinDriver, WiperLock, ZENA and Z-Scale are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

GestIC and ULPP are registered trademarks of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 1997-2014, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

ISBN: 978-1-63276-093-7

*Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.*

**QUALITY MANAGEMENT SYSTEM  
CERTIFIED BY DNV  
= ISO/TS 16949 =**





# MICROCHIP

## Worldwide Sales and Service

### AMERICAS

**Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
<http://www.microchip.com/support>  
Web Address:  
[www.microchip.com](http://www.microchip.com)

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Austin, TX**  
Tel: 512-257-3370

**Boston**  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088

**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Novi, MI  
Tel: 248-848-4000

**Houston, TX**  
Tel: 281-894-5983

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**New York, NY**  
Tel: 631-435-6000

**San Jose, CA**  
Tel: 408-735-9110

**Canada - Toronto**  
Tel: 905-673-0699  
Fax: 905-673-6509

### ASIA/PACIFIC

**Asia Pacific Office**  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9868-6733  
Fax: 61-2-9868-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588  
Fax: 86-23-8980-9500

**China - Hangzhou**  
Tel: 86-571-8792-8115  
Fax: 86-571-8792-8116

**China - Hong Kong SAR**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8473-2460  
Fax: 86-25-8473-2470

**China - Qingdao**  
Tel: 86-532-8502-7355  
Fax: 86-532-8502-7205

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8864-2200  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

### ASIA/PACIFIC

**India - Bangalore**  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-3019-1500

**Japan - Osaka**  
Tel: 81-6-6152-7160  
Fax: 81-6-6152-9310

**Japan - Tokyo**  
Tel: 81-3-6880-3770  
Fax: 81-3-6880-3771

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or  
82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-5778-366  
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830

**Taiwan - Taipei**  
Tel: 886-2-2508-8600  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

### EUROPE

**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Dusseldorf**  
Tel: 49-2129-3766400

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Germany - Pforzheim**  
Tel: 49-7231-424750

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Italy - Venice**  
Tel: 39-049-7625286

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Poland - Warsaw**  
Tel: 48-22-3325737

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**Sweden - Stockholm**  
Tel: 46-8-5090-4654

**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820

03/25/14