TMP1075 Temperature Sensor With I²C and SMBus Interface in Industry Standard LM75 Form Factor and Pinout

1 Features

- Digital Output: SMBus™, I²C
- Compatible to I³C Mixed Fast Mode
- Supports up to 32 Device Addresses
- Alert Pin Function
- Resolution: 12 Bits
- Accuracy:
  - ±2°C (Maximum) from −25°C to +85°C
  - ±3°C (Maximum) from −55°C to +125°C
- Operating Low Quiescent Current: 10-μA (typical)
- Shutdown Low Quiescent Current: 0.3-μA (typical)
- Wide Supply Range: 1.7 V to 3.6 V
- Small 8-Pin Package: VSSOP, SOIC and DFN

2 Applications

- Power-Supply Temperature Monitoring
- Computer Peripheral Thermal Protection
- Notebook Computers
- Cell Phones
- Battery Management
- Office Machines
- Thermostat Controls
- Environmental Monitoring and HVAC
- Electro Mechanical Device Temperature

3 Description

The TMP1075 is a lower power, higher accuracy replacement to the industry standard LM75 and TMP75 digital temperature sensors. Available in SOIC-8 and SOP-8 packages, the TMP1075 offers pin to pin and software compatibility to quickly upgrade any existing xx75 design. New with the TMP1075 is an optional 2x2mm DFN package reducing the PCB footprint by 79% compared to an SOIC package.

The TMP1075 provides a 25% improvement in accuracy over standard xx75 temperature sensors and offers an on-chip 12-bit analog-to digital converter (ADC) providing a temperature resolution of 0.0625°C.

Compatible with SMBus, two-wire, and I²C interfaces, the TMP1075 supports up to 32 devices address and provides SMBus Alert.

The TMP1075 devices are ideal for temperature measurement in a variety of communication, computer, consumer, environmental, industrial, and instrumentation applications.

The TMP1075 devices are specified for operation over a temperature range of −55°C to +125°C.

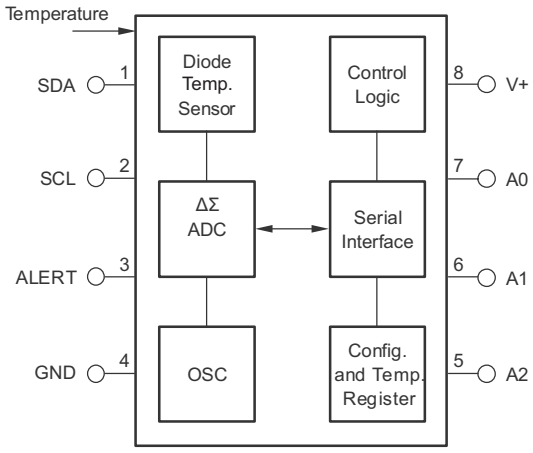
The TMP1075 units are 100% tested on a production setup that is NIST traceable and verified with equipment that is calibrated to ISO/IEC 17025 accredited standards.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP1075	SOIC (8)	4.90 mm × 3.91 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	DFN (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

TMP1075 Internal Block Diagram



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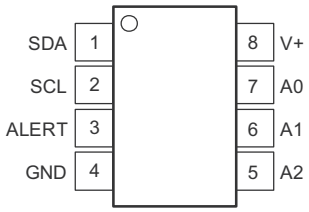
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2018	*	Initial release.

5 Pin Configuration and Functions

DGK and D Packages
8-Pin VSSOP and SOIC
Top View



NOTE: Pin 1 is determined by orienting the package marking as indicated in the diagram.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SDA	I/O	Serial data. Open-drain output; requires a pullup resistor.
2	SCL	I	Serial clock.
3	ALERT	O	Overtemperature alert. Open-drain output; requires a pullup resistor.
4	GND	—	Ground
5	A2	I	Address select A2: Connect to GND or V+
6	A1	I	Address select A1: Connect to GND, V+, SDA or SCL
7	A0	I	Address select A0: Connect to GND, V+, SDA or SCL
8	V+	I	Supply voltage, 1.7 V to 5.5 V

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply, V+		6	V
Input voltage	–0.5	6	V
Input voltage	–0.5	(V+) + 0.5	V
Input current		10	mA
Operating temperature	–55	150	°C
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–60	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2K	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	TBD	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage	1.7		5.5	V
Operating free-air temperature, T_A	–55		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP1075 DGK (SOIC), D (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	202.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	82	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	124.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	17.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	122.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	°C/W
	Thermal Mass	TBD	TBD

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

at T_A = −55°C to +125°C and V+ = 1.7 V to 3.6 V (unless noted); typical specification are at T_A = 25°C and V+=3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE INPUT						
	Range		–55		125	°C
	Accuracy (temperature error)	−25°C to +85°C		±0.5	±2	°C
		−55°C to +125°C		±1	±3	
	Accuracy (temperature error) vs supply	PSRR		0	±0.02	°C/V
	Resolution	1 LSB (12 bit)		0.0625		°C
DIGITAL INPUT/OUTPUT						
	Input capacitance			5		pF
V_{IH}	High-level input logic		0.7(V+)			V
V_{IL}	Low-level input logic		-0.3		0.3(V+)	V
I_{IN}	Leakage input current		-0.1		0.1	µA
	Input voltage hysteresis	SCL and SDA pins		600		mV
V_{OL}	Low-level output logic	I_{OL} = -3 mA, SDA and ALERT pins	0	0.15	0.4	V
	ADC Conversion time	12 bits one-shot mode	4.5	5	5.75	ms
	Conversion Rate	CR1 = 0, CR0 = 0 (default)		27.5		ms
		CR1 = 0, CR0 = 1		55		
		CR1 = 1, CR0 = 0		110		
		CR1 = 1, CR0 = 1		220		
	Sampling Period Precision		-10	5	10	%
	Timeout time		20	25	35	ms
POWER SUPPLY						
	Operating range		1.7	3.3	3.6	V
I_Q	Quiescent current	CR1 = 0, CR0 = 0 (default)		10	16	µA
		CR1 = 0, CR0 = 1		5.5		µA
		CR1 = 1, CR0 = 0		4		
		CR1 = 1, CR0 = 1		2.7		
		During active conversion ,serial bus inactive		52	98	µA
I_{SD}	Shutdown current	Serial bus active, SCL frequency = 400 kHz		13		µA
		Serial bus inactive		0.37	1.5	µA
	POR, Power-on reset threshold	Rising		1.22		V
		Falling		1.1		
	Reset time			0.3		ms

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6.6 Timing Requirements

see the *Timing Diagrams* and *Two-Wire Timing Diagrams* sections for additional information

			FAST MODE		HIGH-SPEED MODE		UNIT
			MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	V+	0.001	0.4	0.001	2.38	MHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	See the *Timing Diagrams* section	1300		160		ns
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.		600		160		ns
$t_{(SUSTA)}$	Repeated START condition setup time		600		160		ns
$t_{(SUSTO)}$	STOP condition setup time		600		160		ns
$t_{(HDDAT)}$	Data hold time		4	900	4	120	ns
$t_{(SUDAT)}$	Data setup time		100		10		ns
$t_{(LOW)}$	SCL clock low period	V+, see the *Timing Diagrams* section	1300		280		ns
$t_{(HIGH)}$	SCL clock high period	See the *Timing Diagrams* section	600		60		ns
t_FD	Data fall time	See the *Timing Diagrams* section		300		150	ns
t_{RC}	Clock rise time	See the *Two-Wire Timing Diagrams* section		300		40	ns
		SCLK ≤ 100 kHz, see the *Timing Diagrams* section		1000			
t_{FC}	Clock fall time	See the *Two-Wire Timing Diagrams* section		300		40	ns

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
t_{LPF}	Spike filter for I^3C compatibility	SCL= 12.5 MHz	50			ns

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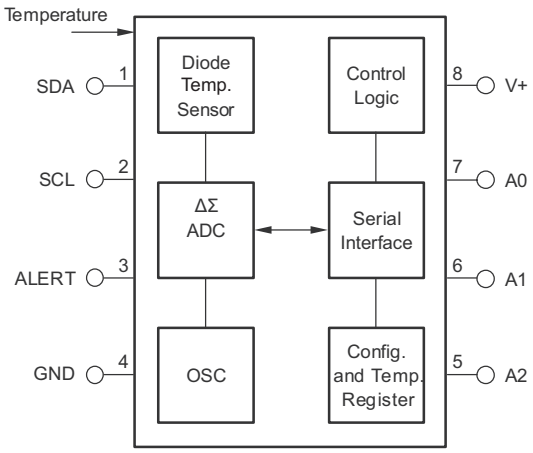
7 Detailed Description

7.1 Overview

The TMP1075 device are digital temperature sensors that are optimal for thermal management and thermal protection applications. The TMP1075 is a two-wire, SMBus, and I^2C interface-compatible. The devices are specified over a temperature range of −40°C to +125°C. The *Functional Block Diagram* section shows an internal block diagram of TMP1075 device.

The temperature sensor in the TMP1075 is the device itself. Thermal paths run through the package leads as well as the plastic package. The package leads provide the primary thermal path because of the lower thermal resistance of the metal.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Digital Temperature Output

The digital output from each temperature measurement conversion is stored in the read-only Temperature register. The Temperature register of the TMP1075 is a 12-bit read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are listed in Table 6 and . The first 12 bits are used to indicate temperature with all remaining bits equal to zero. Data format for temperature is listed in . Negative numbers are represented in binary twos complement format. Following power-up or reset, the Temperature register reads 0°C until the first conversion is complete.

Table 1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
127.9375	0111 1111 1111	7FF
100	0110 0100 0000	640
80	0101 0000 0000	500
75	0100 1011 0000	4B0
50	0011 0010 0000	320
25	0001 1001 0000	190
0.25	0000 0000 0100	004
0.0625	0000 0000 0001	001
0	0000 0000 0000	000
-0.0625	1111 1111 1111	FFF
-0.25	1111 1111 1100	FFC
-25	1110 0111 0000	E70
-50	1100 1110 0000	CE0

7.3.2 Serial Interface

The TMP1075 operate only as slave devices on the SMBus, two-wire, and I^2C interface-compatible bus. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP1075 support the transmission protocol for fast (up to 400 kHz) and high-speed (up to 2 MHz) modes. All data bytes are transmitted MSB first.

7.3.2.1 Bus Overview

The device that initiates the transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated, indicated by pulling the data line (SDA) from a high to low logic level when SCL is high. All slaves on the bus shift in the slave address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an Acknowledge bit. During data transfer SDA must remain stable when SCL is high because any change in SDA when SCL is high is interpreted as a control signal.

When all data are transferred, the master generates a STOP condition indicated by pulling SDA from low to high when SCL is high.

7.3.2.2 Serial Bus Address

To communicate with the TMP1075, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The TMP1075 features three address pins to allow up to 32 devices to be addressed on a single bus interface. describes the pin logic levels used to properly connect up to 32 devices. The state of pins A0, A1, and A2 is sampled on every bus communication and must be set prior to any activity on the interface.

Table 2. Address Pins and Slave Addresses for the TMP1075

A2	A1	A0	ADDRESS, HEX
0	0	SDA	80
0	0	SCL	82
0	1	SDA	84
0	1	SCL	86
1	0	SDA	88
1	0	SCL	8A
1	1	SDA	8C
1	1	SCL	8E
0	0	0	90
0	0	1	92
0	1	0	94
0	1	1	96
1	0	0	98
1	0	1	9A
1	1	0	9C
1	1	1	9E
0	SDA	SDA	A0
0	SDA	SCL	A2
0	SCL	SDA	A4
0	SCL	SCL	A6
1	SDA	SDA	A8
1	SDA	SCL	AA
1	SCL	SDA	AC
1	SCL	SCL	AE
0	SDA	0	B0
0	SDA	1	B2
0	SCL	0	B4
0	SCL	1	B6
1	SDA	0	B8
1	SDA	1	BA
1	SCL	0	BC
1	SCL	1	BE

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7.3.2.3 Writing and Reading to the TMP1075

Accessing a particular register on the TMP1075 device is accomplished by writing the appropriate value to the Pointer register. The value for the Pointer register is the first byte transferred after the slave address byte with the R/W bit low. Every write operation to the TMP1075 requires a value for the Pointer register (see Figure 2).

When reading from the TMP1075 device, the last value stored in the Pointer register by a write operation is used to determine which register is read by a read operation. To change the register pointer for a read operation, a new value must be written to the Pointer register. This action is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the Pointer register byte. No additional data are required. The master can then generate a START condition and send the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. See Figure 4 for details of this sequence. If repeated reads from the same register are desired, the Pointer register bytes do not have to be continually sent because the TMP1075 remember the Pointer register value until the value is changed by the next write operation.

Register bytes are sent MSB first, followed by the LSB.

7.3.2.4 Slave Mode Operations

The TMP1075 can operate as a slave receiver or slave transmitter.

7.3.2.4.1 Slave Receiver Mode

The first byte transmitted by the master is the slave address, with the R/$\overline{W}$ bit low. The TMP1075 then acknowledges reception of a valid address. The next byte transmitted by the master is the Pointer register. The TMP1075 then acknowledges reception of the Pointer register byte. The next byte or bytes are written to the register addressed by the Pointer register. The TMP1075 acknowledge reception of each data byte. The master can terminate data transfer by generating a START or STOP condition.

7.3.2.4.2 Slave Transmitter Mode

The first byte is transmitted by the master and is the slave address, with the R/$\overline{W}$ bit high. The slave acknowledges reception of a valid slave address. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the Pointer register. The master acknowledges reception of the data byte. The next byte transmitted by the slave is the least significant byte. The master acknowledges reception of the data byte. The master can terminate data transfer by generating a Not-Acknowledge on reception of any data byte, or generating a START or STOP condition.

7.3.2.5 SMBus Alert Function

The TMP1075 support the SMBus Alert function. When the TMP1075 is operating in interrupt mode (TM = 1), the ALERT pin of the TMP1075 can be connected as an SMBus Alert signal. When a master senses that an ALERT condition is present on the ALERT line, the master sends an SMBus Alert command (00011001) on the bus. If the ALERT pin of the TMP1075 is active, the devices acknowledge the SMBus Alert command and respond by returning its slave address on the SDA line. The eighth bit (LSB) of the slave address byte indicates if the temperature exceeding T_{HIGH} or falling below T_{LOW} caused the ALERT condition. This bit is high if the temperature is greater than or equal to T_{HIGH}. This bit is low if the temperature is less than T_{LOW}. See Figure 5 for details of this sequence.

If multiple devices on the bus respond to the SMBus Alert command, arbitration during the slave address portion of the SMBus Alert command determine which device clears its ALERT status. If theTMP1075 wins the arbitration, its ALERT pin becomes inactive at the completion of the SMBus Alert command. If the TMP1075 loses the arbitration, its ALERT pin remains active.

7.3.2.6 General Call

The TMP1075 respond to a two-wire general call address (0000000) if the eighth bit is 0. The device acknowledges the general call address and responds to commands in the second byte. If the second byte is 00000100, the TMP1075 latch the status of their address pins, but do not reset. If the second byte is 00000110, the TMP1075 latch the status of their address pins and reset their internal registers to their power-up values.

7.3.2.7 High-Speed Mode

In order for the two-wire bus to operate at frequencies above 400 kHz, the master device must issue an Hs-mode master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP1075 devices do not acknowledge this byte, but do switch their input filters on SDA and SCL and their output filters on SDA to operate in Hs-mode, allowing transfers at up to 2 MHz. After the Hs-mode master code is issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the TMP1075 switch the input and output filter back to fast-mode operation.

7.3.2.8 Time-Out Function

The TMP1075 resets the serial interface if either SCL or SDA is held low for 25 ms (typical) between a START and STOP condition. The TMP1075 releases the bus if it is pulled low and waits for a START condition. To avoid activating the time-out function, a communication speed of at least 1 kHz must be maintained for the SCL operating frequency.

7.3.3 Timing Diagrams

The TMP1075 devices are two-wire, SMBus, and I^{2}C interface-compatible. Figure 1 to Figure 5 describe the various operations on the TMP1075. The following list provides bus definitions. Parameters for Figure 1 are defined in the *Timing Requirements*.

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low when the SCL line is high defines a START condition. Each data transfer is initiated with a START condition.

Stop Data Transfer: A change in the state of the SDA line from low to high when the SCL line is high defines a STOP condition. Each data transfer is terminated with a repeated START or STOP condition.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the transfer of data.

Acknowledge: Each receiving device, when addressed, is obliged to generate an Acknowledge bit. A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the Acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the termination of the data transfer can be signaled by the master generating a Not-Acknowledge on the last byte that is transmitted by the slave.

7.3.4 Two-Wire Timing Diagrams

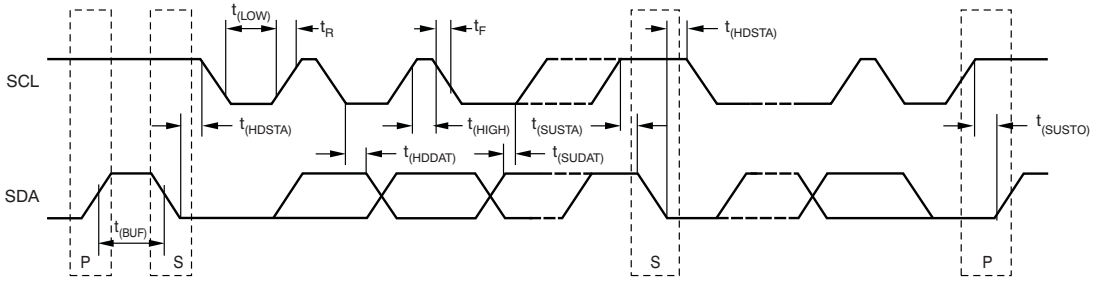

Figure 1. Two-Wire Timing Diagram

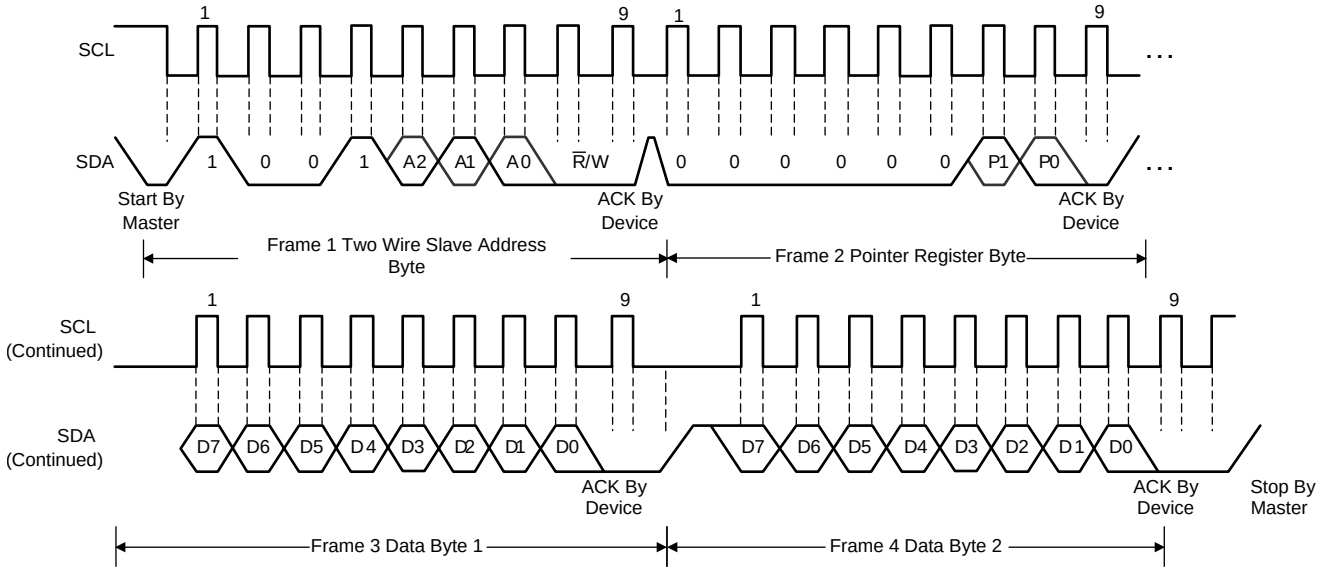

Figure 2. Two-Wire Timing Diagram for the TMP1075 Write Word Format

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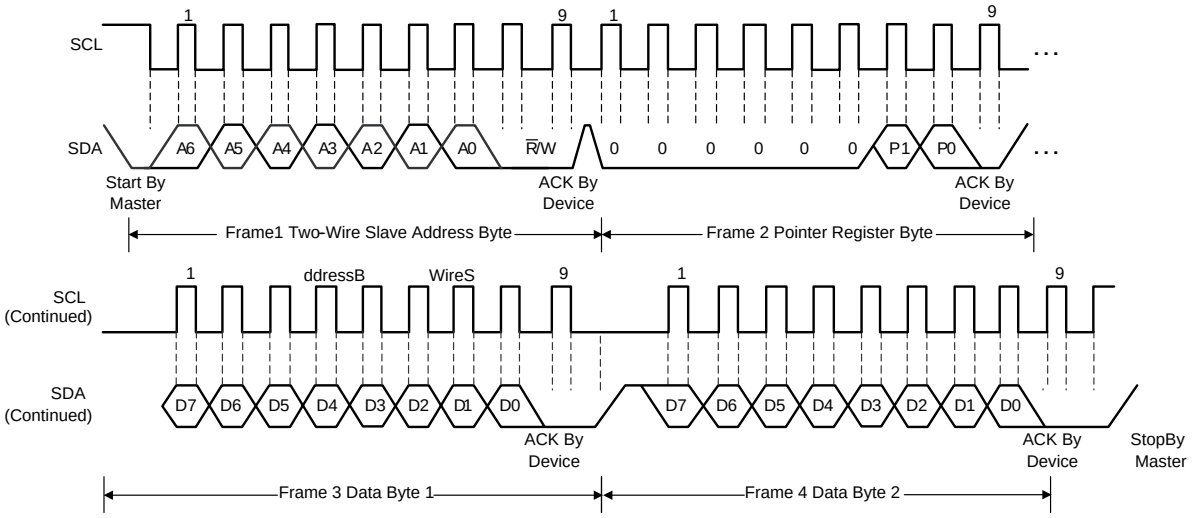
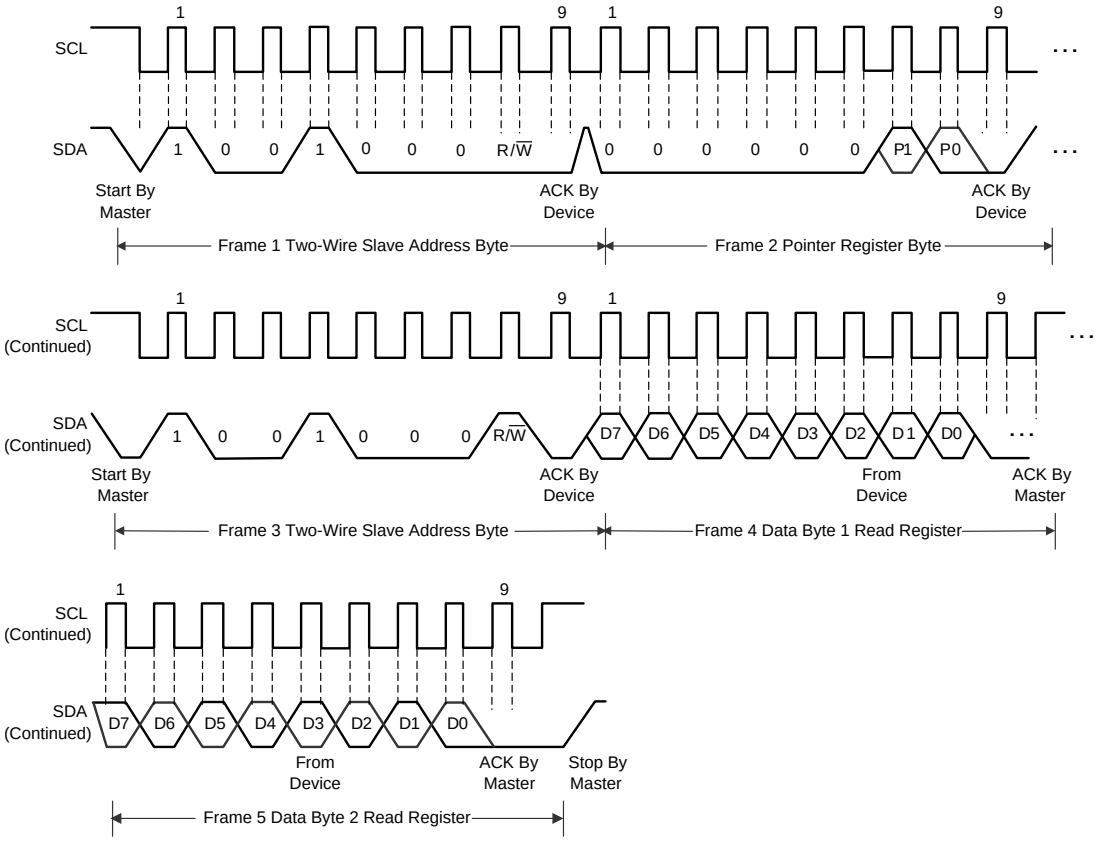


Figure 3. Two-Wire Timing Diagram for the TMP1075 Write Word Format



NOTE: Address pins A0, A1, A2 = 0.

Figure 4. Two-Wire Timing Diagram for Read Word Format

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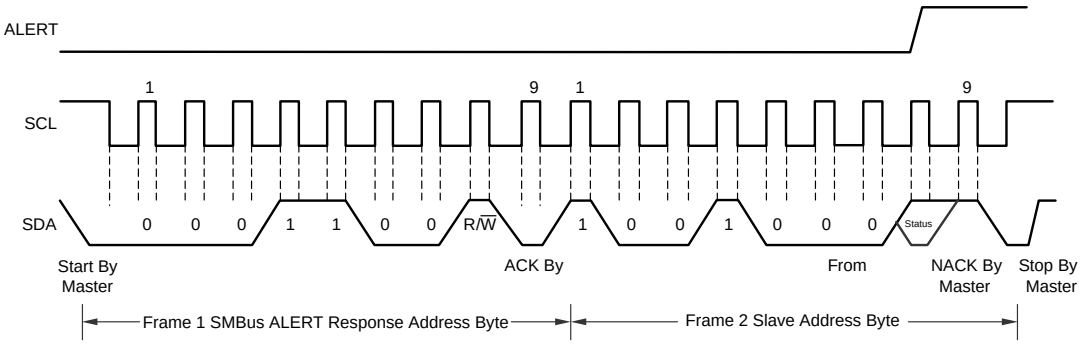

NOTE: Address pins A0, A1, A2 = 0.

Figure 5. Timing Diagram for SMBus ALERT

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7.4 Device Functional Modes

7.4.1 Shutdown Mode (SD)

The shutdown mode of the TMP1075 devices lets the user save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1 μA. Shutdown mode is enabled when the SD bit is 1; the device shuts down when the current conversion is completed. When SD is equal to 0, the device maintains a continuous conversion state.

7.4.2 One-Shot (OS)

The TMP1075 feature a one-shot temperature measurement mode. When the device is in shutdown mode, writing 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP1075 when continuous temperature monitoring is not required. When the configuration register is read, the OS always reads zero.

7.4.3 Thermostat Mode (TM)

The thermostat mode bit of the TMP1075 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High and Low Limit Registers* section.

7.4.4 Comparator Mode (TM = 0)

In comparator mode (TM = 0), the ALERT pin is activated when the temperature equals or exceeds the value in the $T_{(HIGH)}$ register and remains active until the temperature falls below the value in the $T_{(LOW)}$register. For more information on the comparator mode, see the *High and Low Limit Registers* section.

7.4.5 Interrupt Mode (TM = 1)

In interrupt mode (TM = 1), the ALERT pin is activated when the temperature exceeds $T_{(HIGH)}$ or goes below $T_{(LOW)}$ registers. The ALERT pin is cleared when the host controller reads the temperature register. For more information on the interrupt mode, see the *High and Low Limit Registers* section.

7.5 Programming

Table 3. TMP1075 Normal Operation Register Map

PTR	POR			Bit Fields																Description
(hex)	(hex)	ACC	SYM	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	0000	RO	TEMP	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	0	0	0	0	Temperature Result
01	00FF	RW	CFGR	OS	R1	R0	F1	F0	POL	TM	SD	1	1	1	1	1	1	1	1	Configuration
02	4B00	RW	LLIM	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	Temperature Low Limit
03	5000	RW	HLIM	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	0	0	0	0	Temperature High Limit
0F	0075	RO	DIEID	0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	Die ID Register

7.5.1 Pointer Register

Figure 6 shows the internal register structure of the TMP1075. The 8-bit Pointer register of the devices is used to address a given data register. The Pointer register uses the two LSBs to identify which of the data registers must respond to a read or write command. Table 4 identifies the bits of the Pointer register byte. Table 5 describes the pointer address of the registers available in the TMP1075. Power-up reset value of P1/P0 is 00.

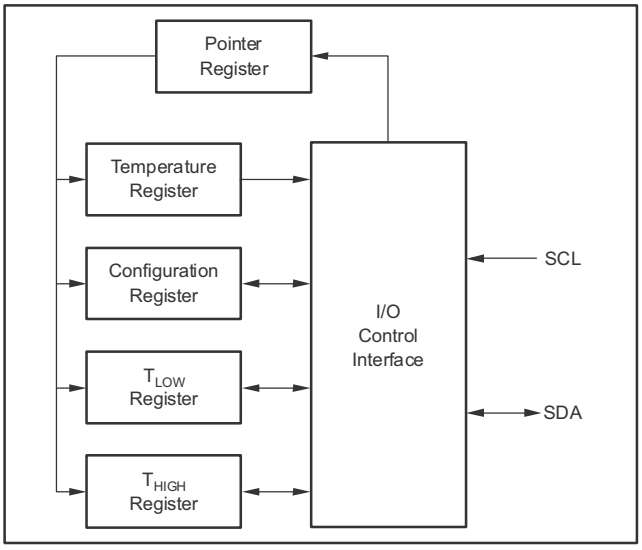

Figure 6. Internal Register Structure of the TMP1075

7.5.1.1 Pointer Register Byte (pointer = N/A) [reset = 00h]

Table 4. Pointer Register Byte

P7	P6	P5	P4	P3	P2	P1	P0
0	0	0	0	0	0	Register Bits	

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7.5.1.2 Pointer Addresses of the TMP1075

Table 5. Pointer Addresses of the TMP1075

P1	P0	TYPE	REGISTER
0	0	R only, default	Temperature register
0	1	R/W	Configuration register
1	0	R/W	T_{LOW} register
1	1	R/W	T_{HIGH} register

7.5.2 Temperature Register

The Temperature register of the TMP1075 is a 12-bit, read-only register that stores the output of the most recent conversion. Two bytes must be read to obtain data, and are described in Table 6 and . The first 12 bits are used to indicate temperature, with all remaining bits equal to zero. The least significant byte does not have to be read if that information is not needed. Following power-up or reset value, the Temperature register reads 0°C until the first conversion is complete.

7.5.2.1 Error Status (ERR) – Read Only

This bit indicates that an error condition has occurred during the conversion and the result is invalid.

0: temperature result is valid and checksum is valid

1: temperature result is invalid and/or checksum is invalid

Table 6. Temperature Register (0x00) [default reset = 0000h]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	0	0	0	0

7.5.3 Configuration Register

The Configuration register is an 16-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read and write operations are performed MSB first. The format of the Configuration register for the TMP1075 is shown in Table 7, followed by a breakdown of the register bits. The power-up or reset value of the Configuration register are all bits equal to 0.

Table 7. Configuration Register Format (0x01) [default reset = 00FFh]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OS	R1	R0	F1	F0	POL	TM	SD	1	1	1	1	1	1	1	1

7.5.3.1 Shutdown Mode (SD)

The shutdown mode of the TMP1075 allows the user to save maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 0.1 μA. Shutdown mode is enabled when the SD bit is 1; the device shuts down immediately after aborting the current conversion. Any write to the Configuration register aborts the current conversion.

7.5.3.2 Thermostat Mode (TM)

The thermostat mode bit of the TMP1075 indicates to the device whether to operate in comparator mode (TM = 0) or interrupt mode (TM = 1). For more information on comparator and interrupt modes, see the *High and Low Limit Registers* section.

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7.5.3.3 Polarity (POL)

The polarity bit of the TMP1075 lets the user adjust the polarity of the ALERT pin output. If the POL bit is set to 0 (default), the ALERT pin becomes active low. When POL bit is set to 1, the ALERT pin becomes active high and the state of the ALERT pin is inverted. The operation of the ALERT pin in various modes is illustrated in Figure 7.

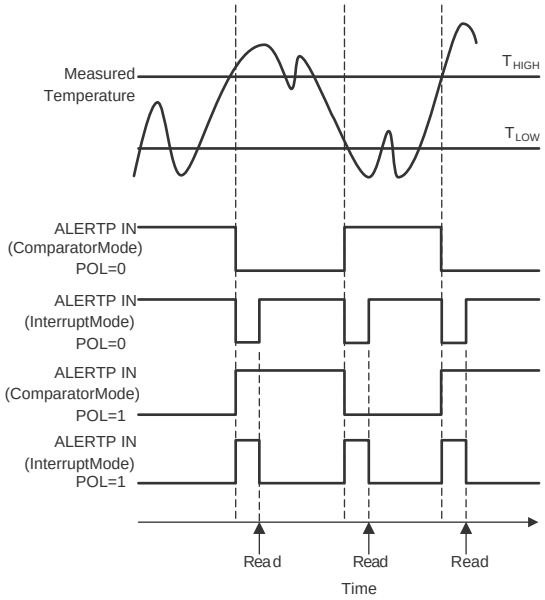

Figure 7. Output Transfer Function Diagrams

7.5.3.4 Fault Queue (F1/F0)

A fault condition is defined as when the measured temperature exceeds the user-defined limits set in the T_{HIGH} and T_{LOW} registers. Additionally, the number of fault conditions required to generate an alert may be programmed using the fault queue. The fault queue is provided to prevent a false alert as a result of environmental noise. The fault queue requires consecutive fault measurements in order to trigger the alert function. Table 8 defines the number of measured faults that can be programmed to trigger an alert condition in the device. For T_{HIGH} and T_{LOW} register format and byte order, see the *High and Low Limit Registers* section.

Table 8. Fault Settings of the TMP1075

F1	F0	CONSECUTIVE FAULTS
0	0	1
0	1	2
1	0	4
1	1	6

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7.5.3.5 Conversion Rate (CR)

The CR bits control the rate of conversion. Table 9 identifies the sampling period.

Table 9. Sampling Period of the TMP1075

CR1	CR0	CONVERSION Rate (Typical)
0	0	27.5 ms
0	1	55 ms
1	0	110 ms
1	1	220 ms

7.5.3.6 One-Shot (OS)

The TMP1075 feature a one-shot temperature measurement mode. When the device is in shutdown mode, writing a 1 to the OS bit starts a single temperature conversion. The device returns to the shutdown state at the completion of the single conversion. This feature is useful to reduce power consumption in the TMP1075 when continuous temperature monitoring is not required. When the configuration register is read, the OS always reads zero.

7.5.4 High and Low Limit Registers

In comparator mode (TM = 0), the ALERT pin of the TMP1075 becomes active when the temperature equals or exceeds the value in T_{HIGH} for a consecutive number of faults according to fault bits F1 and F0. The ALERT pin remains active until the temperature falls below the indicated T_{LOW} value for the same number of faults.

In interrupt mode (TM = 1), the ALERT pin becomes active when the temperature equals or exceeds T_{HIGH} for a consecutive number of fault conditions. the consecutive faults dictated by the F bits also applies to the ALERT due to T_{LOW}. The ALERT pin remains active until a read operation of any register occurs, or the device successfully responds to the SMBus Alert response address. The ALERT pin is also cleared if the device is placed in shutdown mode. When the ALERT pin is cleared, it only become active again by the temperature falling below T_{LOW}. When the temperature falls below T_{LOW}, the ALERT pin becomes active and remains active until cleared by a read operation of any register or a successful response to the SMBus Alert response address. When the ALERT pin is cleared, the above cycle repeats, with the ALERT pin becoming active when the temperature equals or exceeds T_{HIGH}. The ALERT pin can also be cleared by resetting the device with the general call reset command. This action also clears the state of the internal registers in the device by returning the device to comparator mode (TM = 0).

Both operational modes are represented in Figure 7. Table 11, , Table 10, and describe the format for the T_{HIGH} and T_{LOW} registers. The most significant byte is sent first, followed by the least significant byte. Power-up reset values for T_{HIGH} and $_{TLOW}$ are:

T_{HIGH} = 80°C and T_{LOW} = 75°C

The format of the data for T_{HIGH} and T_{LOW} is the same as for the Temperature register.

Table 10. Byte 1 of the T_{LOW} Register (0x03)[default reset = 5000h]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0

Table 11. Byte 1 of the T_{HIGH} Register (0x02) [default reset = 4B00h]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	0	0	0	0

7.5.5 Die ID Register (0x0F)

The Die ID register of the MSB bit reads the static 0x75 hex to indicating device name for TMP1075 as illustrated below.

Table 12. Die ID Register (0x0F) [default reset = 7500h]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP1075 device are used to measure the PCB temperature of the location it is mounted. The TMP1075 feature SMBus, two-wire, and I^2C interface compatibility, with the TMP1075 allowing up to 32 devices on one bus and the TMP1075 allowing up to eight devices on one bus. The TMP1075 feature an SMBus Alert function. The TMP1075 require no external components for operation except for pullup resistors on SCL, SDA, and ALERT, although a 0.1-µF bypass capacitor is recommended.

The sensing device of the TMP1075 device is the device itself. Thermal paths run through the package leads as well as the plastic package. The lower thermal resistance of metal causes the leads to provide the primary thermal path.

8.2 Typical Application

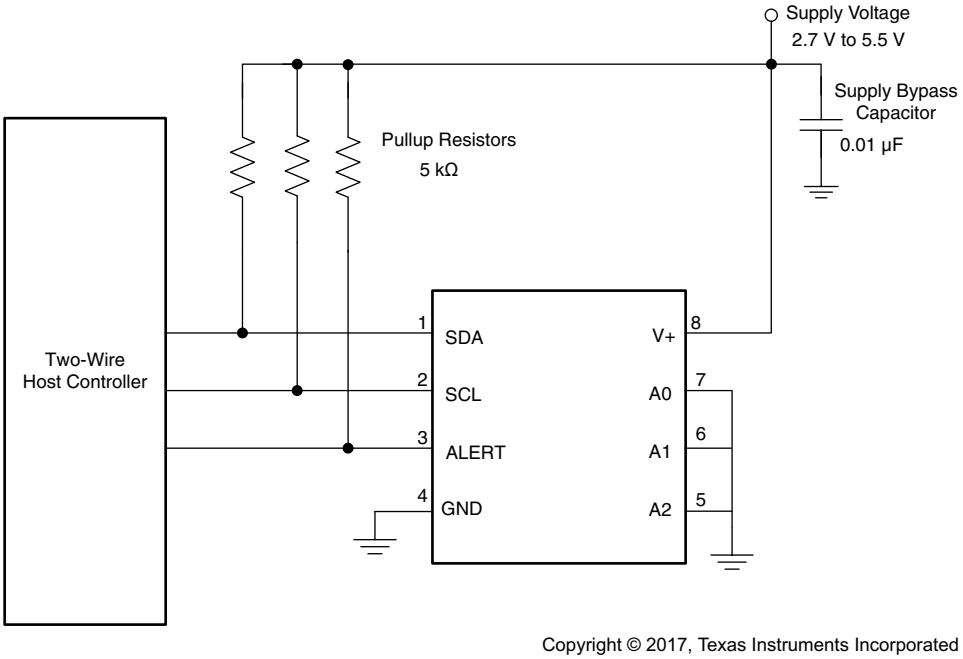

Figure 8. Typical Connections of the TMP1075

8.2.1 Design Requirements

The TMP1075 devices requires pullup resistors on the SCL, SDA, and ALERT pins. The recommended value for the pullup resistor is 5 kΩ. In some applications the pullup resistor can be lower or higher than 5 kΩ but must not exceed 3 mA of current on the SCL and SDA pins, and must not exceed 4 mA on the ALERT pin. A 0.1-µF bypass capacitor is recommended, as shown in Figure 8. The SCL, SDA, and ALERT lines can be pulled up to a supply that is equal to or higher than V_S through the pullup resistors.

ADVANCE INFORMATION

Typical Application (continued)

8.2.2 Detailed Design Procedure

Place the TMP1075 device in close proximity to the heat source that must be monitored, with a proper layout for good thermal coupling. This placement ensures that temperature changes are captured within the shortest possible time interval. To maintain accuracy in applications that require air or surface temperature measurement, take care to isolate the package and leads from ambient air temperature. A thermally-conductive adhesive is helpful in achieving accurate surface temperature measurement.

8.2.3 Application Curve

shows the step response of the TMP1075 device to a submersion in an oil bath of 100ºC from room temperature (27ºC). The time-constant, or the time for the output to reach 63% of the input step, is 1.5 s. The time-constant result depends on the printed-circuit-board (PCB) that the TMPx175 devices are mounted. For this test, the TMP1075 device were soldered to a two-layer PCB that measured 0.375 inch × 0.437 inch.

9 Power Supply Recommendations

The TMP1075 operate with a power supply in the range of 1.7 V to 3.6 V. A power-supply bypass capacitor is required for stability; place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.01 μF. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise.

10 Layout

10.1 Layout Guidelines

Place the power-supply bypass capacitor as close as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.01 μF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. Pull up the open-drain output pins SDA , SCL, and ALERT through 5-kΩ pullup resistors.

10.2 Layout Example

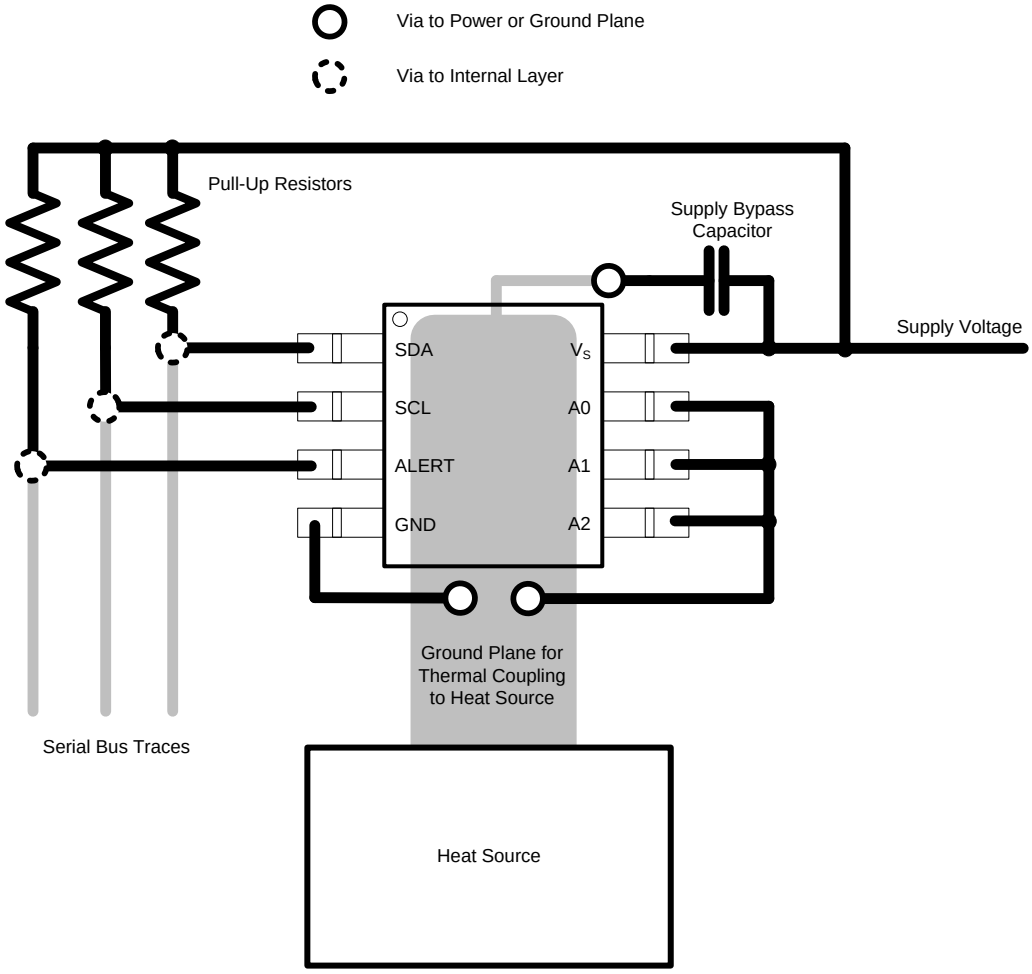

Figure 9. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMP1075DGKT	ACTIVE	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		Samples
TMP1075DGKR	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		
TMP1075DGKT	PREVIEW	VSSOP	DGK	8	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

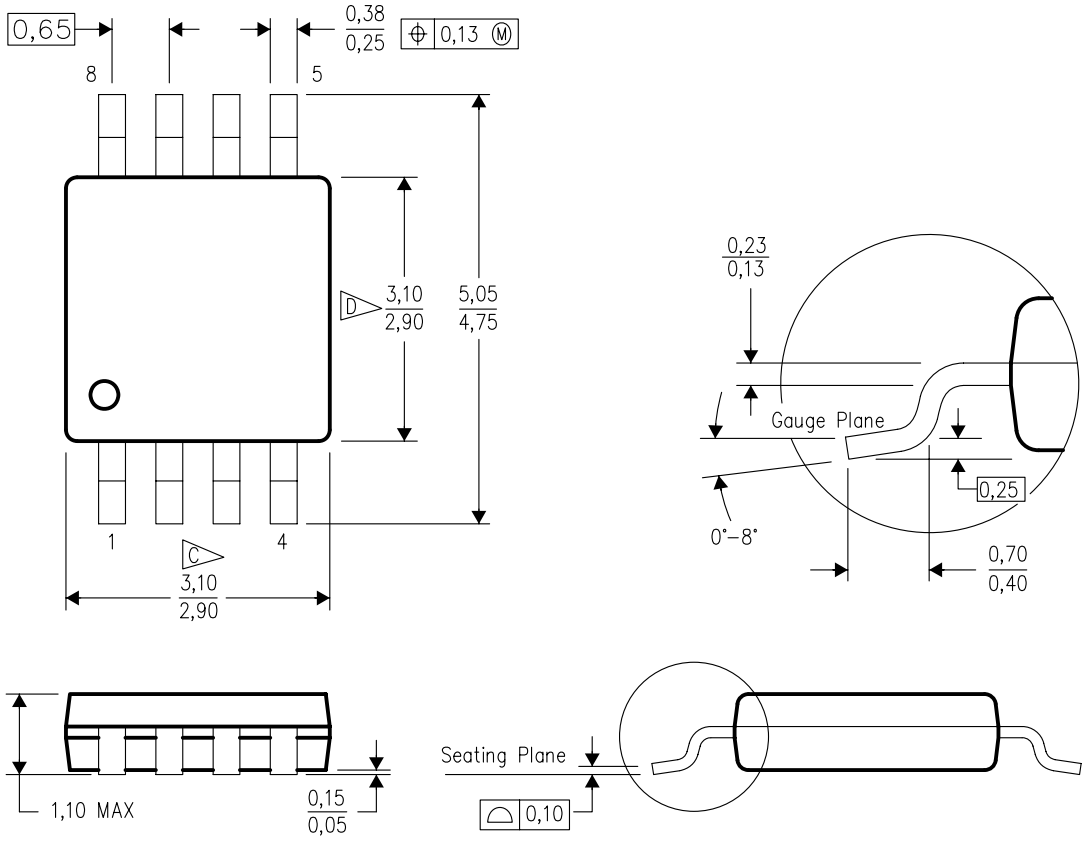
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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