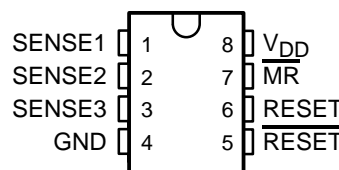


- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Triple Supervisory Circuits for DSP and Processor-Based Systems**
- **Power-On Reset Generator with Fixed Delay Time of 200 ms, No External Capacitor Needed**
- **Temperature-Compensated Voltage Reference**
- **Maximum Supply Current of 40 μA**
- **Supply Voltage Range . . . 2 V to 6 V**
- **Defined $\overline{\text{RESET}}$ Output from $V_{\text{DD}} \geq 1.1 \text{ V}$**
- **SO-8 Package**

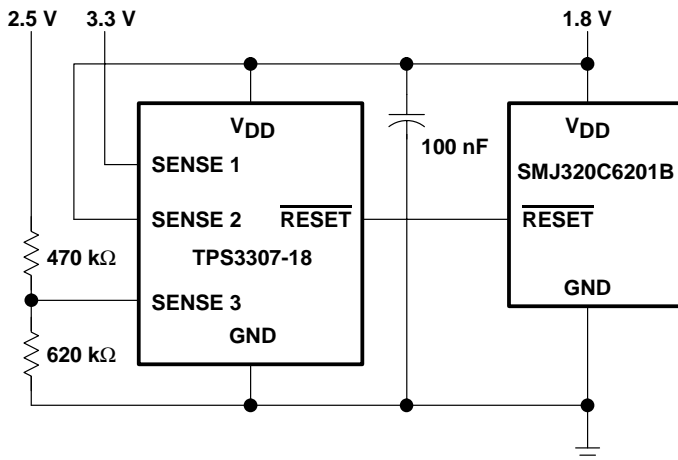
† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**D PACKAGE
(TOP VIEW)**



typical applications

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers TPS3307–18 and SMJ320C6201B.



- **Military applications using DSPs, Microcontrollers or Microprocessors**
- Industrial Equipment**
- Programmable Controls**
- Military Systems**

Figure 1. Applications Using the TPS3307-18

description

The TPS3307-18 is a micropower supply voltage supervisor designed for circuit initialization primarily in automotive DSP and processor-based systems, which require more than one supply voltage.

The TPS3307-18 is designed for monitoring three independent supply voltages: 3.3 V/1.8 V/adj,. The adjustable SENSE input allows the monitoring of any supply voltage >1.25 V.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TPS3307-18-EP TRIPLE PROCESSOR SUPERVISORS

SGLS140 – NOVEMBER 2002

description (continued)

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE			THRESHOLD VOLTAGE (TYP)		
	SENSE1	SENSE2	SENSE3	SENSE1	SENSE2	SENSE3
TPS3307-18	3.3 V	1.8 V	User defined	2.93 V	1.68 V	1.25 V†

† The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors the SENSEn inputs and keeps $\overline{\text{RESET}}$ active as long as SENSEn remain below the threshold voltage V_{IT+} .

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d,typ} = 200$ ms, starts after all SENSEn inputs have risen above the threshold voltage V_{IT+} . When the voltage at any SENSE input drops below the threshold voltage V_{IT-} , the $\overline{\text{RESET}}$ output becomes active (low) again.

The TPS3307-18 incorporates a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. In addition to the active-low $\overline{\text{RESET}}$ output, the TPS3307-18 includes an active-high RESET output.

The device is available in a standard 8-pin SO package, and is characterized for operation over a temperature range of -55°C to 125°C .

ORDERING INFORMATION

TA	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-55°C to 125°C	Small Outline (D)	Tape and Reel	TPS3307-18MDREP	30718E

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

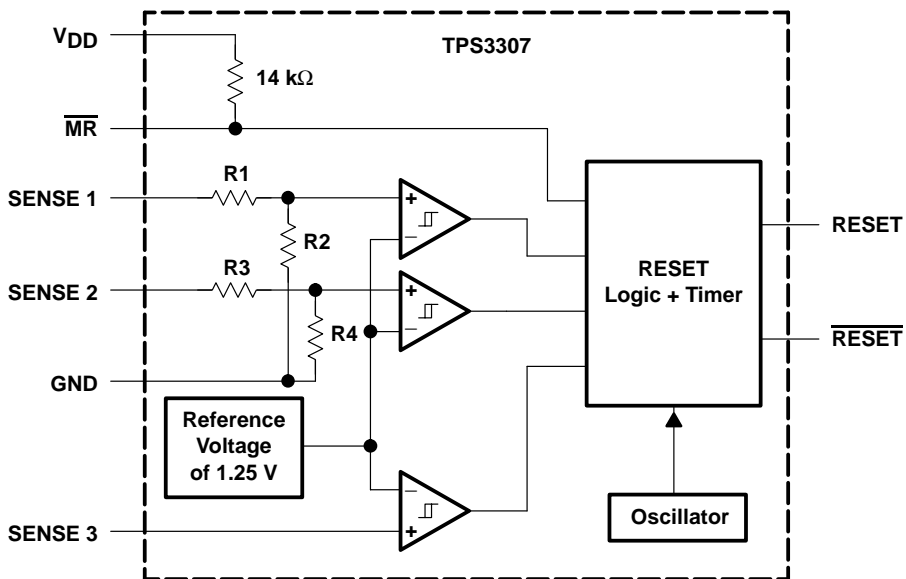
FUNCTION/TRUTH TABLES

$\overline{\text{MR}}$	SENSE1> V_{IT1}	SENSE2> V_{IT2}	SENSE3> V_{IT3}	$\overline{\text{RESET}}$	RESET
L	X	X	X	L	H
H	0	0	0	L	H
H	0	0	1	L	H
H	0	1	0	L	H
H	0	1	1	L	H
H	1	0	0	L	H
H	1	0	1	L	H
H	1	1	0	L	H
H	1	1	1	H	L

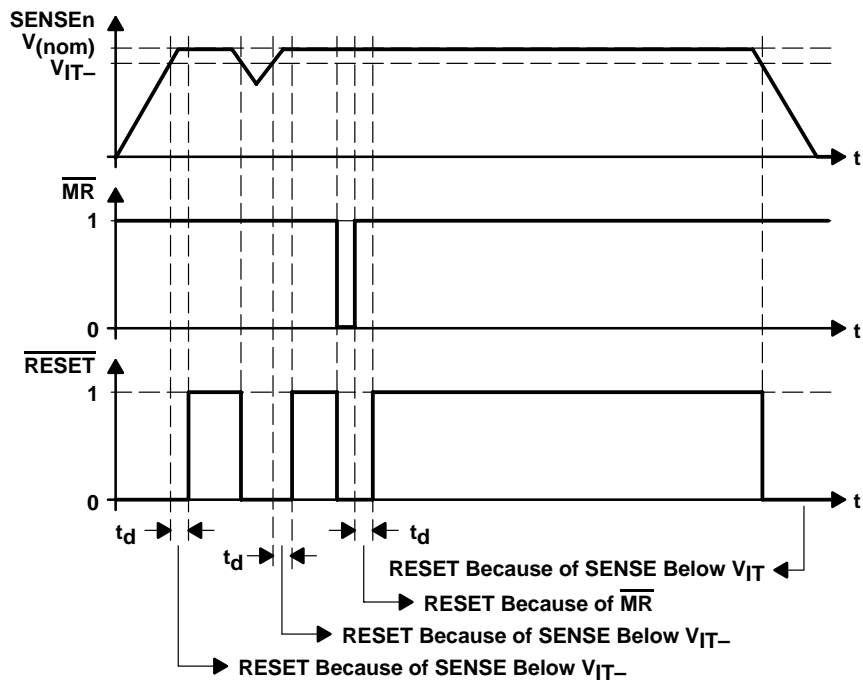
X = Don't care



functional block diagram



timing diagram



TPS3307-18-EP

TRIPLE PROCESSOR SUPERVISORS

SGLS140 – NOVEMBER 2002

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1)	7 V
All other pins (see Note 1)	-0.3 V to 7 V
Maximum low output current, I_{OL}	5 mA
Maximum high output current, I_{OH}	-5 mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	± 20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	-55°C to 125°C
Storage temperature range, T_{stg} (see Note 2)	-65°C to 150°C
Soldering temperature	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be operated at 7 V for more than $t = 1000$ h continuously.

NOTE 2: Long-term, high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See <http://www.ti.com/sc/ep> for more information.

recommended operating conditions at specified temperature range

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage at \overline{MR} and SENSE3, V_I	0	$V_{DD}+0.3$	V
Input voltage at SENSE1 and SENSE2, V_I	0	$(V_{DD}+0.3)V_{IT}/1.25V$	V
High-level input voltage at \overline{MR} , V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage at \overline{MR} , V_{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at \overline{MR} , $\Delta t/\Delta V$		50	ns/V
Operating free-air temperature range, T_A	-55	125	°C



electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V _{OH}	High-level output voltage	V _{DD} = 2 V to 6 V, I _{OH} = -20 μA	V _{DD} - 0.2V			V	
		V _{DD} = 3.3 V, I _{OH} = -2 mA	V _{DD} - 0.4V				
		V _{DD} = 6 V, I _{OH} = -3 mA	V _{DD} - 0.4V				
V _{OL}	Low-level output voltage	V _{DD} = 2 V to 6 V, I _{OL} = 20 μA	0.2			V	
		V _{DD} = 3.3 V, I _{OL} = 2 mA	0.4				
		V _{DD} = 6 V, I _{OL} = 3 mA	0.4				
Power-up reset voltage (see Note 2)		V _{DD} ≥ 1.1 V, I _{OL} = 20 μA	0.4			V	
V _{IT-}	Negative-going input threshold voltage (see Note 3)	VSENSE3	V _{DD} = 2 V to 6 V	1.2	1.25	1.29	V
		VSENSE2		1.6	1.68	1.73	V
		VSENSE1		2.8	2.93	3.02	
V _{hys}	Hysteresis at VSENSEn input	V _{IT-} = 1.25 V	2	10	30	mV	
		V _{IT-} = 1.68 V	2	15	40		
		V _{IT-} = 2.93 V	3	30	60		
I _H	High-level input current	$\overline{\text{MR}}$	MR = 0.7 × V _{DD} , V _{DD} = 6 V		-130	-180	μA
		SENSE1	VSENSE1 = V _{DD} = 6 V		5	8	
		SENSE2	VSENSE2 = V _{DD} = 6 V		6	9	
		SENSE3	VSENSE3 = V _{DD}		-1	1	
I _L	Low-level input current	$\overline{\text{MR}}$	MR = 0 V, V _{DD} = 6 V		-430	-600	μA
		SENSEn	VSENSE1,2,3 = 0 V		-1	1	
I _{DD}	Supply current				40	μA	
C _i	Input capacitance	V _I = 0 V to V _{DD}		10		pF	

- NOTES: 3. The lowest supply voltage at which RESET becomes active. t_r, V_{DD} ≥ 15 μs/V
 4. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1 μF) should be placed close to the supply terminals.

TPS3307-18-EP

TRIPLE PROCESSOR SUPERVISORS

SGLS140 – NOVEMBER 2002

timing requirements at $V_{DD} = 2\text{ V to }6\text{ V}$, $R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	$V_{SENSEnL} = V_{IT-} - 0.2\text{ V}$, $V_{SENSEnH} = V_{IT+} + 0.2\text{ V}$	6	10		μs
		$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100	150		ns

switching characteristics at $V_{DD} = 2\text{ V to }6\text{ V}$, $R_L = 1\text{ M}\Omega$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time	$V_I(\text{SENSEn}) \geq V_{IT+} + 0.2\text{ V}$, $\overline{\text{MR}} \geq 0.7 \times V_{DD}$. See timing diagram	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ $\overline{\text{MR}}$ to $\overline{\text{RESET}}$		200	600	ns
t_{PLH}	Propagation (delay) time, low-to-high level output	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ $\overline{\text{MR}}$ to $\overline{\text{RESET}}$				
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{\text{RESET}}$		1	5	μs
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $\overline{\text{RESET}}$				



TYPICAL CHARACTERISTICS

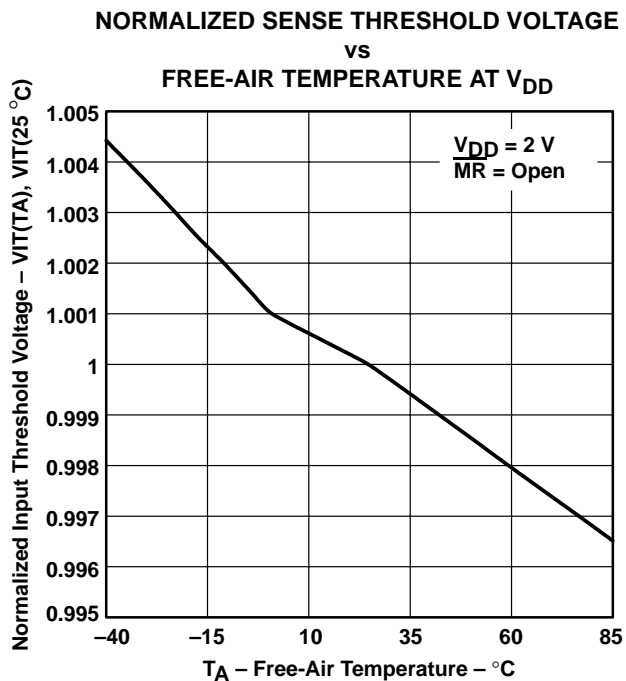


Figure 2

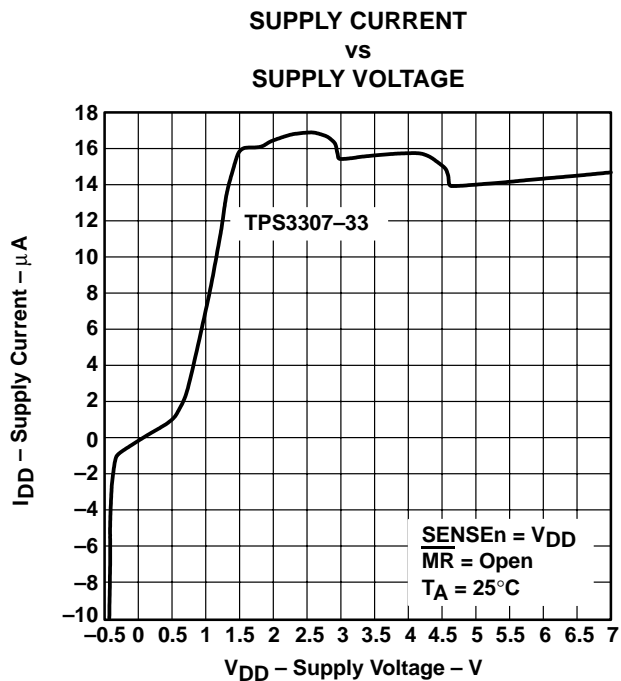


Figure 3

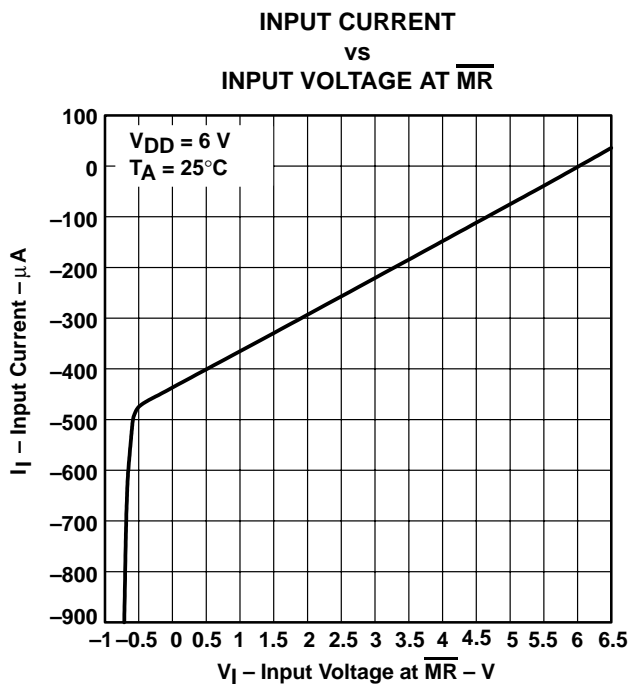


Figure 4

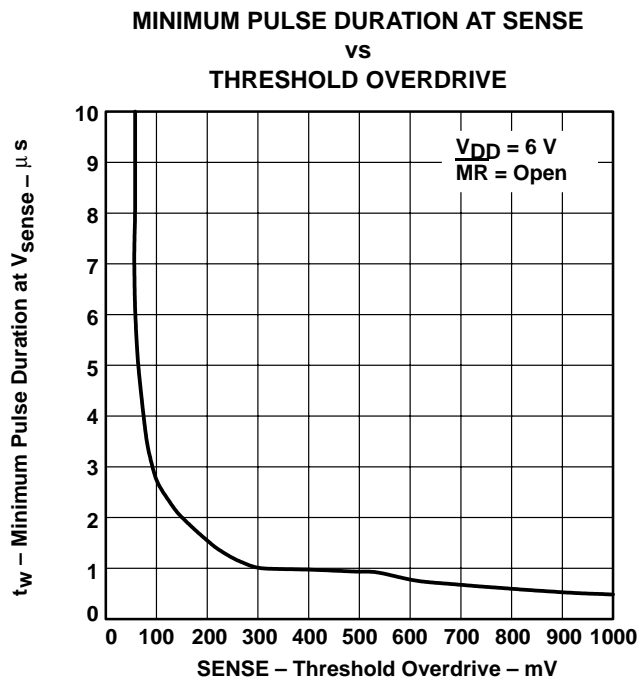


Figure 5

TYPICAL CHARACTERISTICS

**HIGH-LEVEL OUTPUT VOLTAGE
 vs
 HIGH-LEVEL OUTPUT CURRENT**

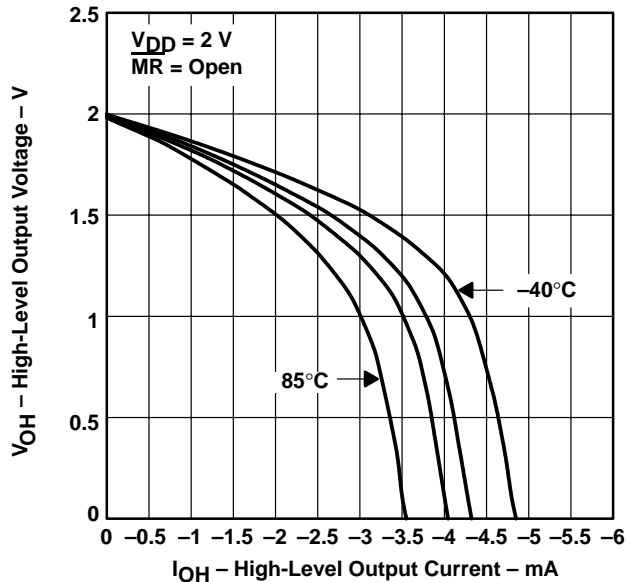


Figure 6

**HIGH-LEVEL OUTPUT VOLTAGE
 vs
 HIGH-LEVEL OUTPUT CURRENT**

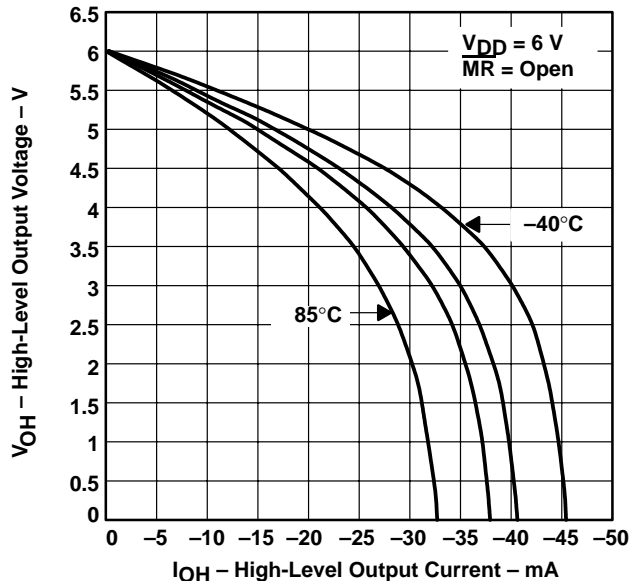


Figure 7

**LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT**

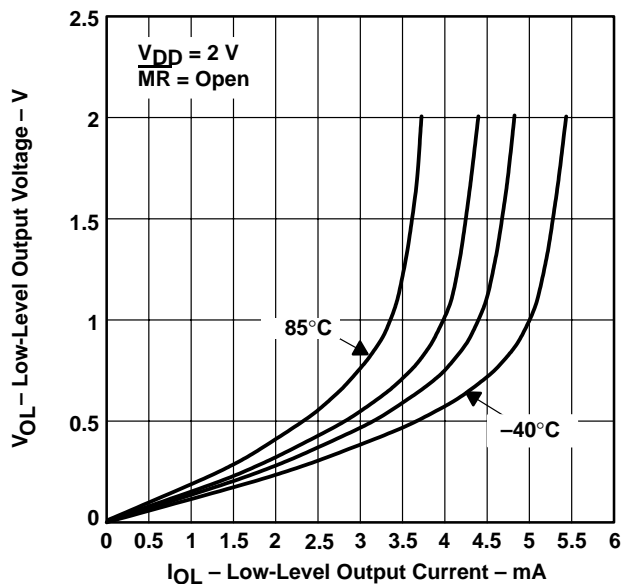


Figure 8

**LOW-LEVEL OUTPUT VOLTAGE
 vs
 LOW-LEVEL OUTPUT CURRENT**

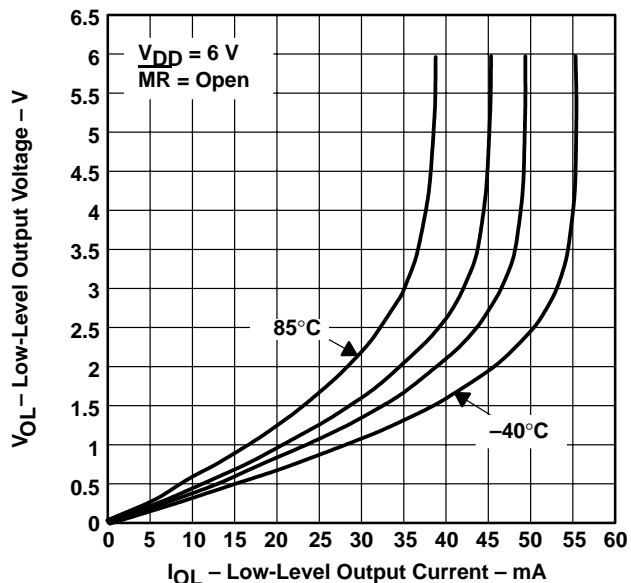


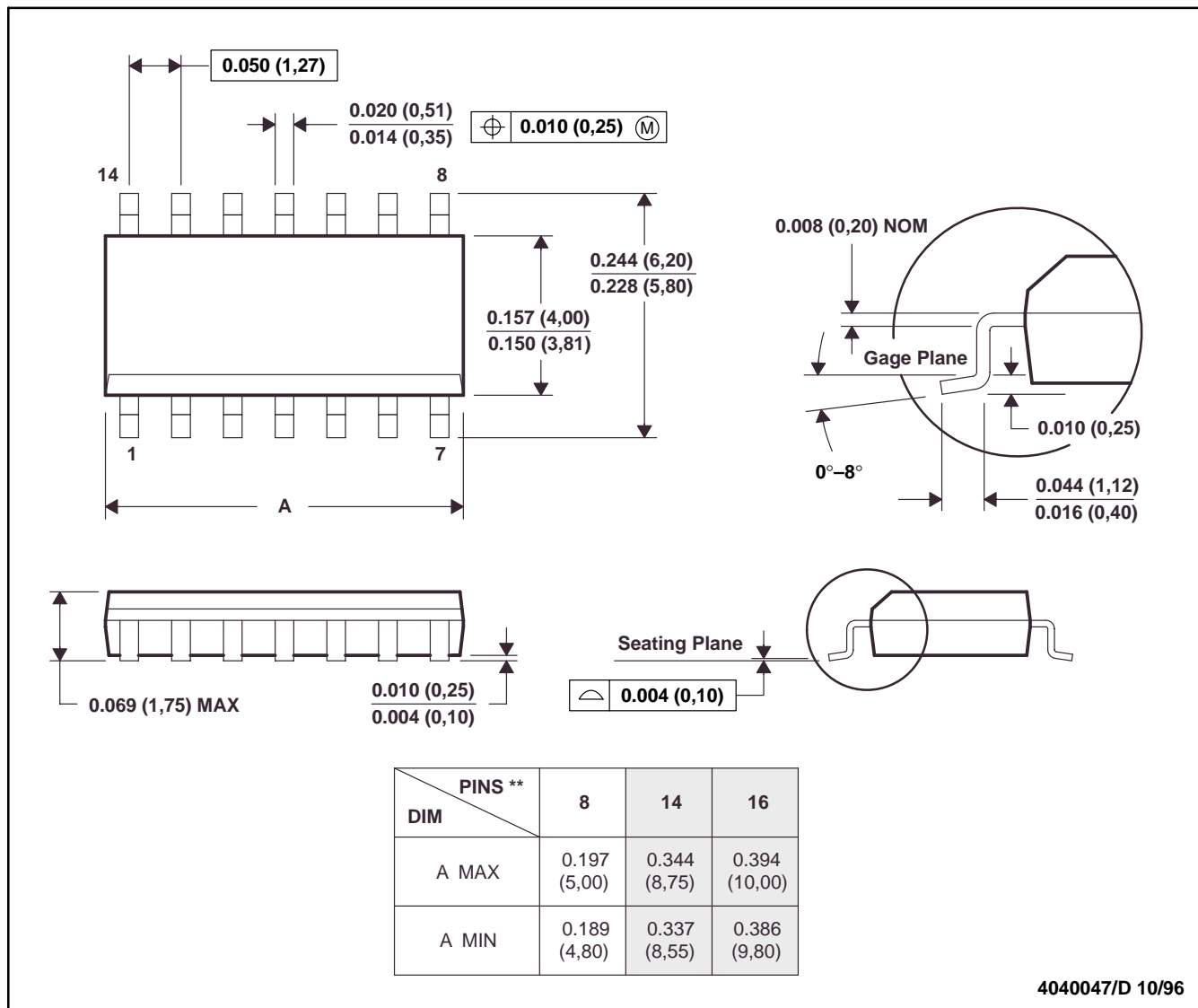
Figure 9

MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265