

SN54AS867, SN54AS869 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

- Fully Programmable With Synchronous Counting and Loading
- SN74ALS867A and 'AS867 Have Asynchronous Clear; SN74ALS869 and 'AS869 Have Synchronous Clear
- Fully Independent Clock Circuit Simplifies Use
- Ripple-Carry Output for n-Bit Cascading
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

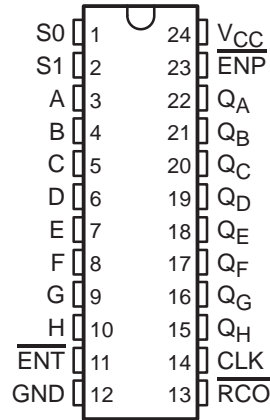
These synchronous, presettable, 8-bit up/down counters feature internal-carry look-ahead circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the count-enable ($\overline{\text{ENP}}$, $\overline{\text{ENT}}$) inputs and internal gating. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters. A buffered clock (CLK) input triggers the eight flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; they may be preset to any number between 0 and 255. The load-input circuitry allows parallel loading of the cascaded counters. Because loading is synchronous, selecting the load mode disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

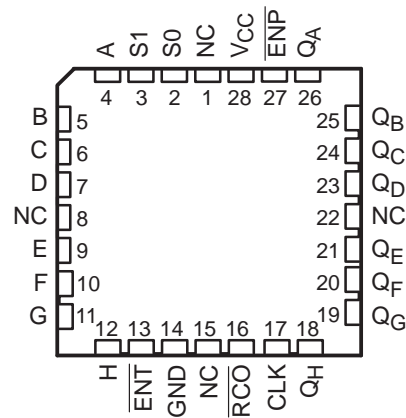
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Two count-enable ($\overline{\text{ENP}}$ and $\overline{\text{ENT}}$) inputs and a ripple-carry ($\overline{\text{RCO}}$) output are instrumental in accomplishing this function. Both $\overline{\text{ENP}}$ and $\overline{\text{ENT}}$ must be low to count. The direction of the count is determined by the levels of the select (S0, S1) inputs as shown in the function table. $\overline{\text{ENT}}$ is fed forward to enable $\overline{\text{RCO}}$. $\overline{\text{RCO}}$ thus enabled produces a low-level pulse while the count is zero (all outputs low) counting down or 255 counting up (all outputs high). This low-level overflow-carry pulse can be used to enable successive cascaded stages. Transitions at $\overline{\text{ENP}}$ and $\overline{\text{ENT}}$ are allowed regardless of the level of CLK. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. With the exception of the asynchronous clear on the SN74ALS867A and 'AS867, changes at S0 and S1 that modify the operating mode have no effect on the Q outputs until clocking occurs. For the 'AS867 and 'AS869, any time $\overline{\text{ENP}}$ and/or $\overline{\text{ENT}}$ is taken high, $\overline{\text{RCO}}$ either goes or remains high. For the SN74ALS867A and SN74ALS869, any time $\overline{\text{ENT}}$ is taken high, $\overline{\text{RCO}}$ either goes or remains high. The function of the counter (whether enabled, disabled, loading, or counting) is dictated solely by the conditions meeting the stable setup and hold times.

SN54AS867, SN54AS869 . . . JT PACKAGE
SN74ALS867A, SN74ALS869, SN74AS867,
SN74AS869 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS867, SN54AS869 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

description (continued)

The SN54AS867 and SN54AS869 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS867A, SN74ALS869, SN74AS867, and SN74AS869 are characterized for operation from 0°C to 70°C .

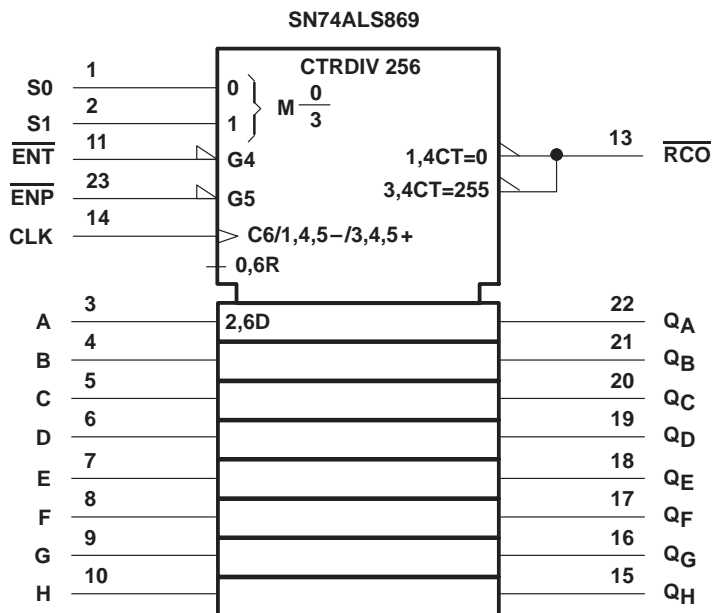
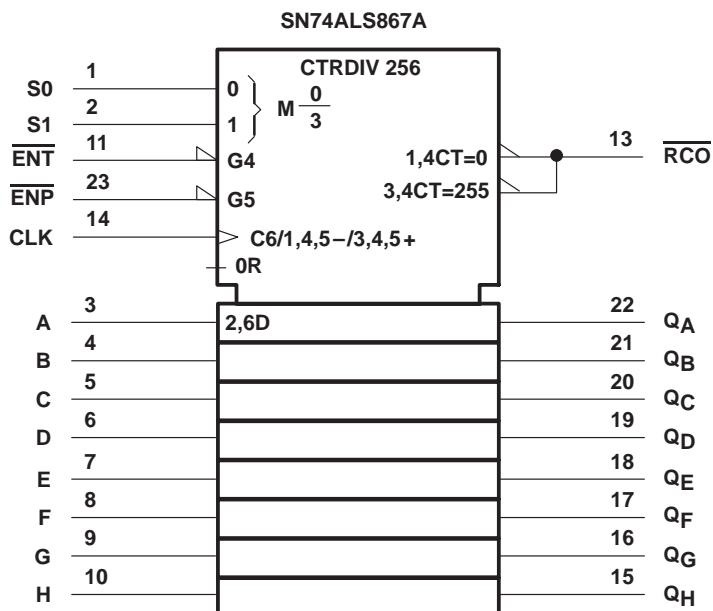
FUNCTION TABLE

| S1 | S0 | FUNCTION |
|-----------|-----------|-----------------|
| L | L | Clear |
| L | H | Count down |
| H | L | Load |
| H | H | Count up |

SN54AS867, SN54AS869
 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

logic symbols†

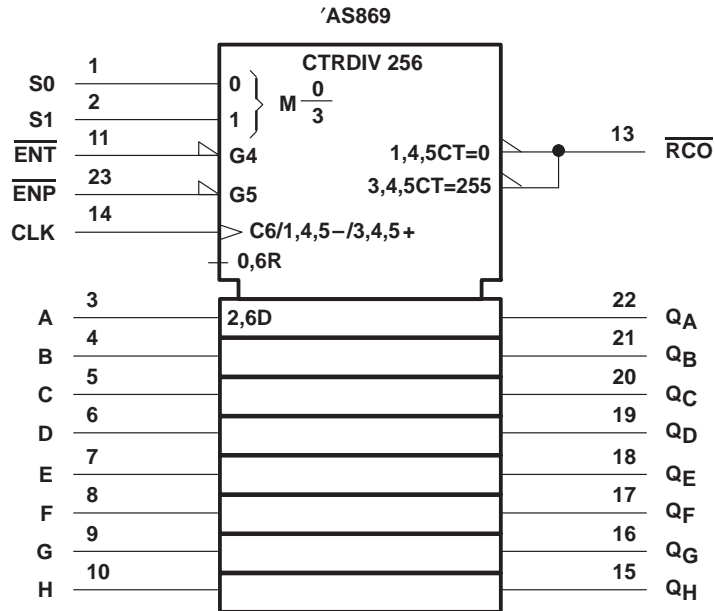
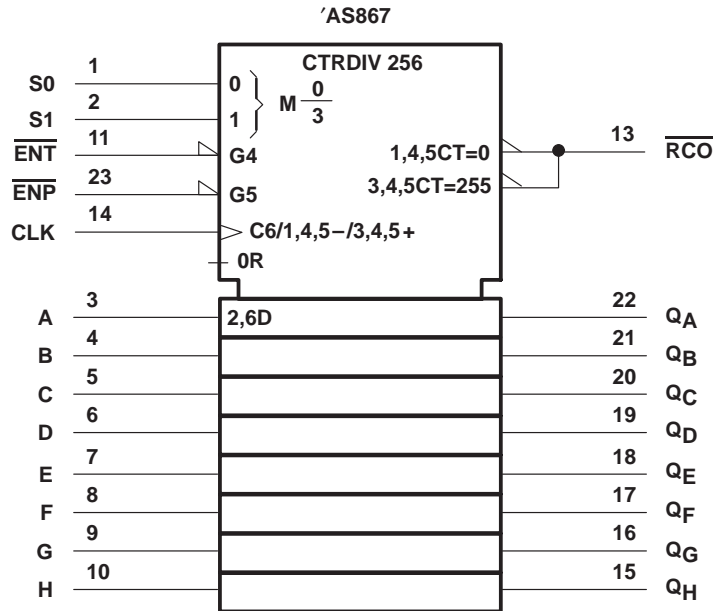


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the DW, JT, and NT packages.

SN54AS867, SN54AS869
 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

logic symbols (continued)†

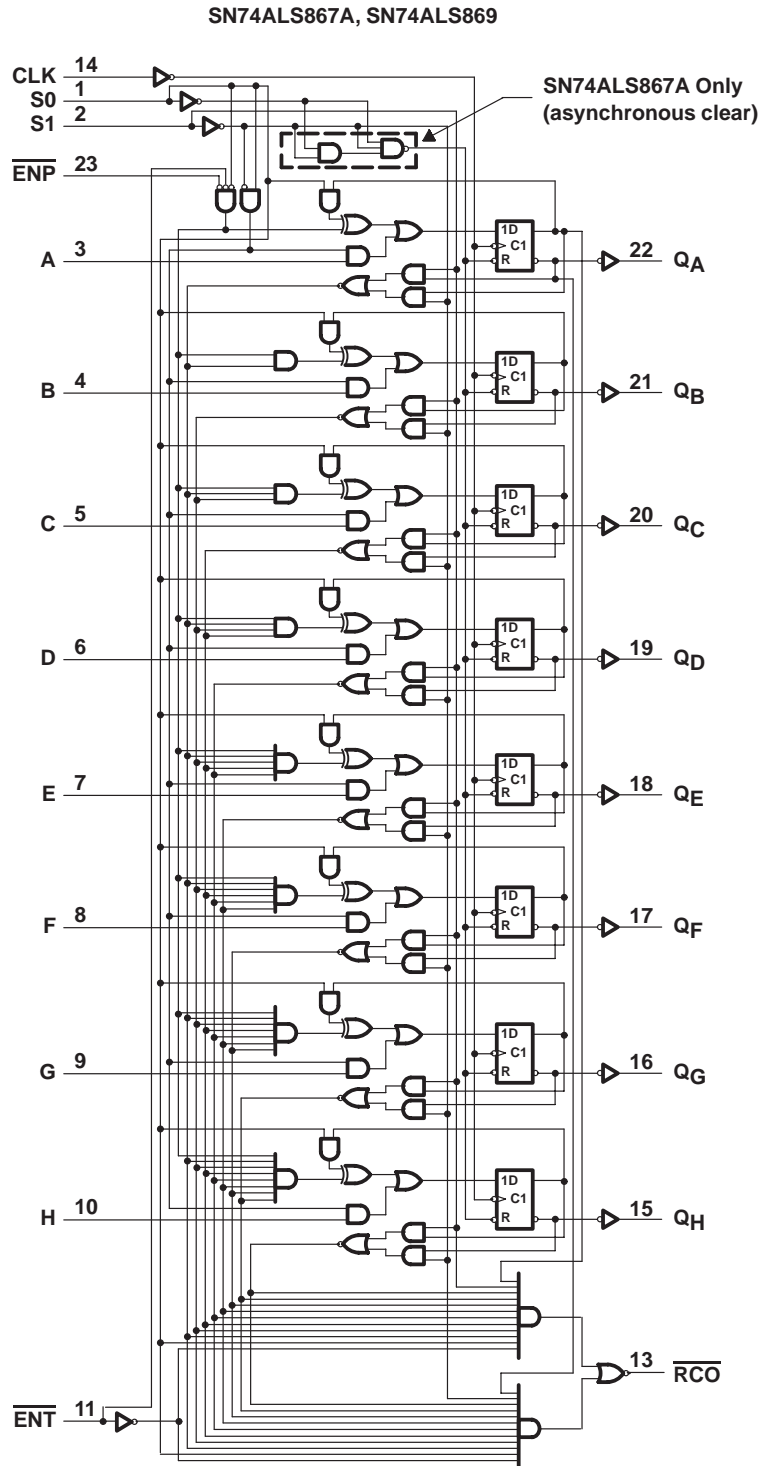


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for the DW, JT, and NT packages.

SN54AS867, SN54AS869
 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

logic diagram (positive logic)

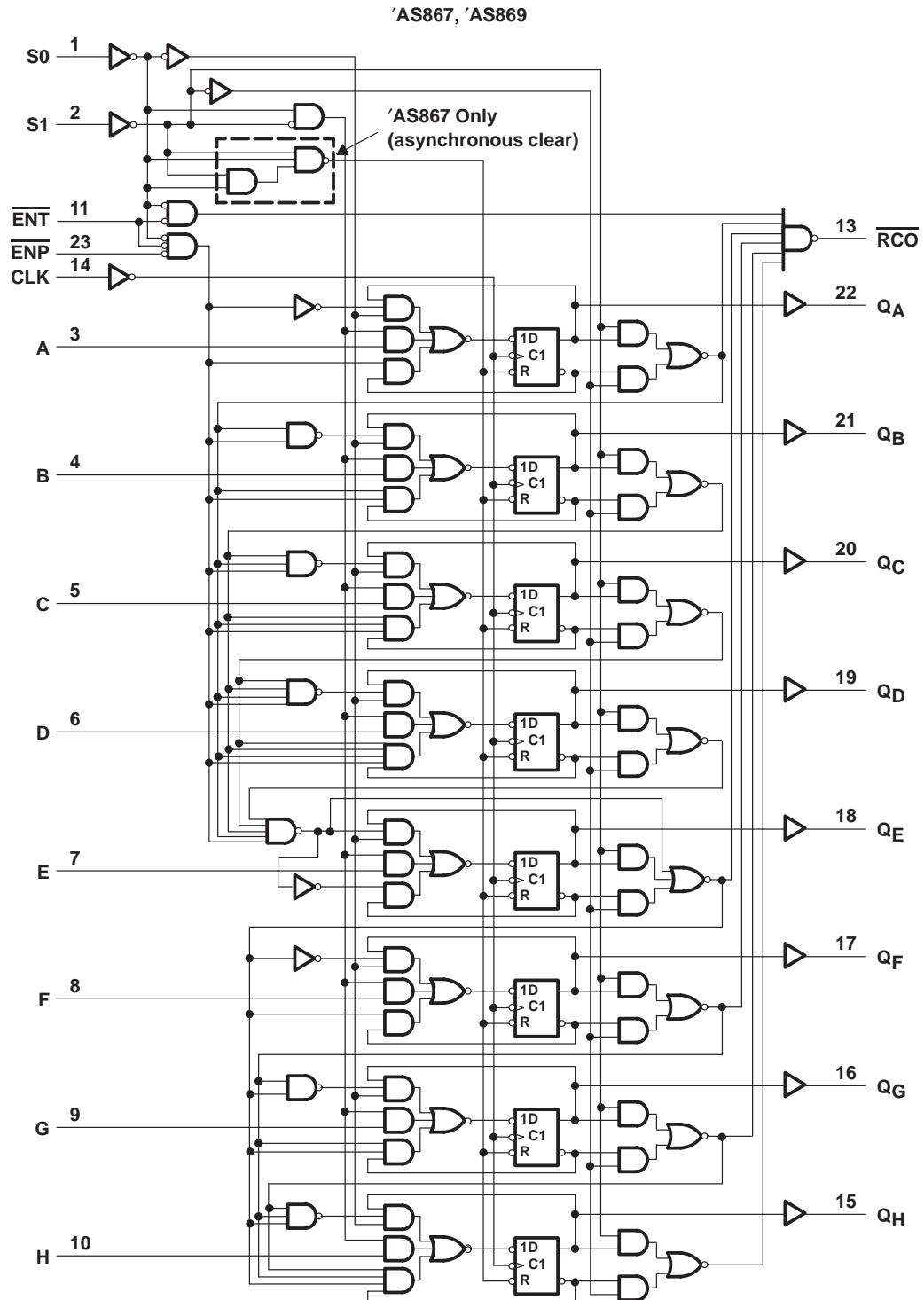


Pin numbers shown are for the DW, JT, and NT packages.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

logic diagram (positive logic)



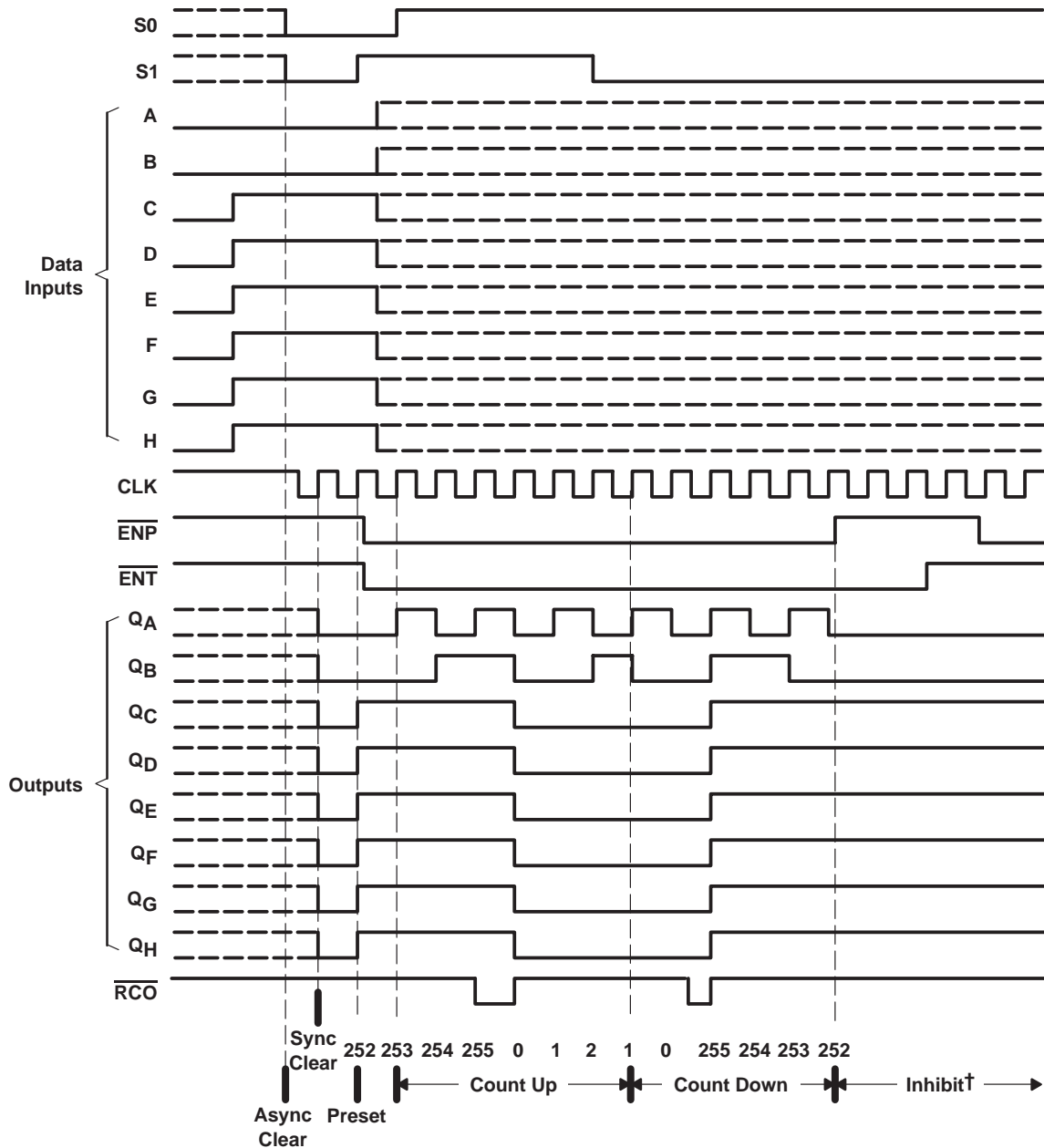
Pin numbers shown are for the DW, JT, and NT packages.



typical clear, preset, count, and inhibit sequences

The following sequence is illustrated below:

1. Clear outputs to zero (SN74ALS867A and 'AS867 are asynchronous;
 SN74ALS869 and 'AS869 are synchronous.)
2. Preset to binary 252
3. Count up to 253, 254, 255, 0, 1, and 2
4. Count down to 1, 0, 255, 254, 253, and 252
5. Inhibit



† ENT and ENP both must be low for counting to occur.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN74ALS867A | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN74ALS867A | | | UNIT |
|----------------|--|--|-----|------|------|
| | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | -0.4 | mA |
| I_{OL} | Low-level output current | | | 8 | mA |
| f_{clock} | Clock frequency | 0 | | 35 | MHz |
| $t_{w(clock)}$ | Pulse duration, CLK high or low | 14 | | | ns |
| $t_{w(clear)}$ | Pulse duration of clear pulse, S0 and S1 low | 10 | | | ns |
| t_{su} | Setup time before CLK↑ | Data inputs A–H | 10 | | ns |
| | | \overline{ENP} or \overline{ENT} | 15 | | |
| | | S0 low and S1 high (load) | 12 | | |
| | | S0 high and S1 low (count down) | 12 | | |
| | | S0 and S1 high (count up) | 12 | | |
| t_h | Hold time after CLK↑ | S0 high after S1↑ or S1 high after S0↑ | 3 | | ns |
| | | Data inputs A–H | 0 | | |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN74ALS867A | | | UNIT |
|-----------|---|-----------------|------|------|------|
| | | MIN | TYP‡ | MAX | |
| V_{IK} | $V_{CC} = 4.5 V$, $I_I = -18 mA$ | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5 V$ to $5.5 V$, $I_{OH} = -0.4 mA$ | $V_{CC} - 2$ | | | V |
| V_{OL} | $V_{CC} = 4.5 V$ | $I_{OL} = 4 mA$ | 0.25 | 0.4 | V |
| | | $I_{OL} = 8 mA$ | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5 V$, $V_I = 7 V$ | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5 V$, $V_I = 2.7 V$ | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5 V$, $V_I = 0.4 V$ | | | -0.2 | mA |
| $I_{O§}$ | $V_{CC} = 5.5 V$, $V_O = 2.25 V$ | -30 | | -112 | mA |
| I_{CC} | $V_{CC} = 5.5 V$ | | 28 | 45 | mA |

‡ All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



SN54AS867, SN54AS869
 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
 SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX† | | UNIT |
|------------------|-----------------------------|-------------------------|---|-----|------|
| | | | SN74ALS867A | | |
| | | | MIN | MAX | |
| f _{max} | | | 35 | | MHz |
| t _{PLH} | CLK | $\overline{\text{RCO}}$ | 4 | 14 | ns |
| t _{PHL} | | | 4 | 14 | |
| t _{PLH} | CLK | Any Q | 3 | 16 | ns |
| t _{PHL} | | | 3 | 16 | |
| t _{PLH} | $\overline{\text{ENT}}$ | $\overline{\text{RCO}}$ | 3 | 14 | ns |
| t _{PHL} | | | 2 | 9 | |
| t _{PHL} | S0 or S1 (clear mode) | Any Q | 8 | 26 | ns |
| t _{PLH} | S0 or S1 (count up/down) | $\overline{\text{RCO}}$ | 4 | 16 | ns |
| t _{PHL} | | | 4 | 16 | |
| t _{PLH} | S0 or S1 (clear mode) | $\overline{\text{RCO}}$ | 4 | 16 | ns |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN74ALS869 | 0°C to 70°C |
| Storage temperature range | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN74ALS869 | | | UNIT |
|----------------|---------------------------------|--|-----|------|------|
| | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | V |
| I_{OH} | High-level output current | | | –0.4 | mA |
| I_{OL} | Low-level output current | | | 8 | mA |
| f_{clock} | Clock frequency | 0 | | 35 | MHz |
| $t_{w(clock)}$ | Pulse duration, CLK high or low | 14 | | | ns |
| t_{su} | Setup time before CLK↑ | Data inputs A–H | 10 | | ns |
| | | \overline{ENP} or \overline{ENT} | 15 | | |
| | | S0 and S1 low (clear) | 13 | | |
| | | S0 low and S1 high (load) | 13 | | |
| | | S0 high and S1 low (count down) | 13 | | |
| | | S0 and S1 high (count up) | 13 | | |
| t_h | Hold time after CLK↑ | S0 high after S1↑ or S1 high after S0↑ | 3 | | ns |
| | | Data inputs A–H | 0 | | |
| T_A | Operating free-air temperature | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN74ALS869 | | | UNIT |
|--------------|---|------------------------|------|------|------|
| | | MIN | TYP‡ | MAX | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | –1.2 | V |
| V_{OH} | $V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$ | $V_{CC} - 2$ | | | V |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | $I_{OL} = 4\text{ mA}$ | 0.25 | 0.4 | V |
| | | $I_{OL} = 8\text{ mA}$ | 0.35 | 0.5 | |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$ | | | 0.1 | mA |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | | | 20 | μA |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$ | | | –0.2 | mA |
| I_{O}^{\S} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | –30 | | –112 | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | | 28 | 45 | mA |

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .



SN54AS867, SN54AS869
 SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX† | | UNIT |
|------------------|-----------------------|------------------|---|-----|------|
| | | | SN74ALS869 | | |
| | | | MIN | MAX | |
| f _{max} | | | 35 | | MHz |
| t _{PLH} | CLK | \overline{RCO} | 4 | 14 | ns |
| t _{PHL} | | | 4 | 14 | |
| t _{PLH} | CLK | Any Q | 3 | 16 | ns |
| t _{PHL} | | | 3 | 16 | |
| t _{PLH} | \overline{ENT} | \overline{RCO} | 3 | 14 | ns |
| t _{PHL} | | | 2 | 9 | |
| t _{PLH} | S1 (count up/down) | \overline{RCO} | 4 | 15 | ns |
| t _{PHL} | | | 4 | 15 | |
| t _{PLH} | S0 (clear/load) | \overline{RCO} | 4 | 16 | ns |
| t _{PHL} | | | 4 | 12 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN54AS867 | –55°C to 125°C |
| SN74AS867 | 0°C to 70°C |
| Storage temperature range | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN54AS867 | | | SN74AS867 | | | UNIT |
|------------------|--|--------------------------------------|-----|-----|-----------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.8 | | | 0.8 | V |
| I_{OH} | High-level output current | | | –2 | | | –2 | mA |
| I_{OL} | Low-level output current | | | 20 | | | 20 | mA |
| f_{clock}^* | Clock frequency | 0 | | 40 | 0 | | 50 | MHz |
| $t_{w(clock)}^*$ | Pulse duration, CLK high or low | 12.5 | | | 10 | | | ns |
| $t_{w(clear)}^*$ | Pulse duration of clear pulse, S0 and S1 low | 12.5 | | | 10 | | | ns |
| t_{su}^* | Setup time before CLK↑ | Data inputs A–H | 5 | | 4 | | | ns |
| | | \overline{ENP} or \overline{ENT} | 9 | | 8 | | | |
| | | S0 low and S1 high (load) | 11 | | 10 | | | |
| | | S0 and S1 low (clear) | 11 | | 10 | | | |
| | | S0 high and S1 low (count down) | 42 | | 40 | | | |
| | | S0 and S1 high (count up) | 42 | | 40 | | | |
| t_h^* | Hold time after CLK↑ | | | 0 | | | 0 | ns |
| t_{skew}^* | Skew time between S0 and S1 (maximum to avoid inadvertent clear) | | | 8 | | | 7 | ns |
| T_A | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | SN54AS867 | | SN74AS867 | | UNIT | | |
|-----------------|---|--------------|--|-----------|--------------|------|---------------|-----|
| | | MIN | TYP† | MAX | MIN | | TYP† | MAX |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | -1.2 | V | |
| V_{OH} | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$ | $V_{CC} - 2$ | | | $V_{CC} - 2$ | | V | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | | $I_{OL} = 20\text{ mA}$, V_{IL} on $\overline{ENT} = 0.7\text{ V}$ | 0.34 | 0.5 | | V | |
| | | | | | | 0.34 | | 0.5 |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$ | | | 0.1 | | 0.1 | mA | |
| I_{IH} | $V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$ | | | 40 | | 40 | μA | |
| | | | | 20 | | 20 | | |
| I_{IL} | $V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$ | | | -4 | | -4 | mA | |
| | | | | -2 | | -2 | | |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$ | -30 | | -112 | | -30 | -112 | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$ | | 134 | 195 | | 134 | 195 | mA |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_L = 500\ \Omega$, $T_A = \text{MIN to MAX}\S$ | | | | UNIT |
|-------------|----------------------|------------------|---|-----|-----------|-----|------|
| | | | SN54AS867 | | SN74AS867 | | |
| | | | MIN | MAX | MIN | MAX | |
| f_{max}^* | | | 40 | | 50 | | MHz |
| t_{PLH} | CLK | \overline{RCO} | 5 | 31 | 5 | 22 | ns |
| t_{PHL} | | | 6 | 19 | 6 | 16 | |
| t_{PLH} | CLK | Any Q | 3 | 12 | 3 | 11 | ns |
| t_{PHL} | | | 4 | 16 | 4 | 15 | |
| t_{PLH} | \overline{ENT} | \overline{RCO} | 3 | 19 | 3 | 10 | ns |
| t_{PHL} | | | 5 | 21 | 5 | 17 | |
| t_{PLH} | \overline{ENP} | \overline{RCO} | 5 | 16 | 5 | 14 | ns |
| t_{PHL} | | | 5 | 21 | 5 | 17 | |
| t_{PHL} | Clear (S0 or S1 low) | Any Q | 7 | 23 | 7 | 21 | ns |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|----------------|
| Supply voltage, V_{CC} | 7 V |
| Input voltage, V_I | 7 V |
| Operating free-air temperature range, T_A : SN54AS869 | –55°C to 125°C |
| SN74AS869 | 0°C to 70°C |
| Storage temperature range | –65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

| | | SN54AS869 | | | SN74AS869 | | | UNIT |
|-----------------------|---------------------------------|--------------------------------------|-----|-----|-----------|-----|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | 0.7 | | | 0.8 | V |
| I_{OH} | High-level output current | | | –2 | | | –2 | mA |
| I_{OL} | Low-level output current | | | 20 | | | 20 | mA |
| f_{clock}^* | Clock frequency | | | 40 | | | 45 | MHz |
| $t_w(\text{clock})^*$ | Pulse duration, CLK high or low | 12.5 | | | 11 | | | ns |
| t_{su}^* | Setup time before CLK↑ | Data inputs A–H | 6 | | 5 | | | ns |
| | | \overline{ENP} or \overline{ENT} | 10 | | 9 | | | |
| | | S0 low and S1 high (load) | 13 | | 11 | | | |
| | | S0 and S1 low (clear) | 13 | | 11 | | | |
| | | S0 high and S1 low (count down) | 52 | | 50 | | | |
| | | S0 and S1 high (count up) | 52 | | 50 | | | |
| t_h^* | Hold time after CLK↑ | | | 0 | | | 0 | ns |
| T_A | Operating free-air temperature | –55 | | 125 | 0 | | 70 | °C |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54AS867, SN54AS869
SN74ALS867A, SN74ALS869, SN74AS867, SN74AS869
SYNCHRONOUS 8-BIT UP/DOWN COUNTERS

SDAS115C – DECEMBER 1982 – REVISED JANUARY 1995

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SN54AS869 | | SN74AS869 | | UNIT | |
|------------------|-------------------------|---|--|------|---------------------|------|------|------|
| | | | MIN | TYP† | MAX | MIN | | TYP† |
| V _{IK} | | V _{CC} = 4.5 V, I _I = -18 mA | | | -1.2 | | | V |
| V _{OH} | | V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA | | | V _{CC} - 2 | | V | |
| | | V _{CC} = 4.5 V, I _{OH} = -2 mA | V _{CC} - 2* | | | | | |
| V _{OL} | $\overline{\text{RCO}}$ | V _{CC} = 4.5 V | I _{OL} = 20 mA, V _{IL} on $\overline{\text{ENT}}$ = 0.7 V | 0.34 | 0.5 | | | V |
| | Other outputs | | | | | 0.34 | 0.5 | |
| I _I | | V _{CC} = 5.5 V, V _I = 7 V | | | 0.1 | 0.1 | | mA |
| I _{IH} | $\overline{\text{ENT}}$ | V _{CC} = 5.5 V, V _I = 2.7 V | | | 40 | 40 | | μA |
| | Other inputs | | | | 20 | 20 | | |
| I _{IL} | $\overline{\text{ENT}}$ | V _{CC} = 5.5 V, V _I = 0.4 V | | | -4 | -4 | | mA |
| | Other inputs | | | | -2 | -2 | | |
| I _O ‡ | | V _{CC} = 5.5 V, V _O = 2.25 V | -30 | -112 | -30 | -112 | | mA |
| I _{CC} | | V _{CC} = 5.5 V | 134 | 195 | 134 | 195 | | mA |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

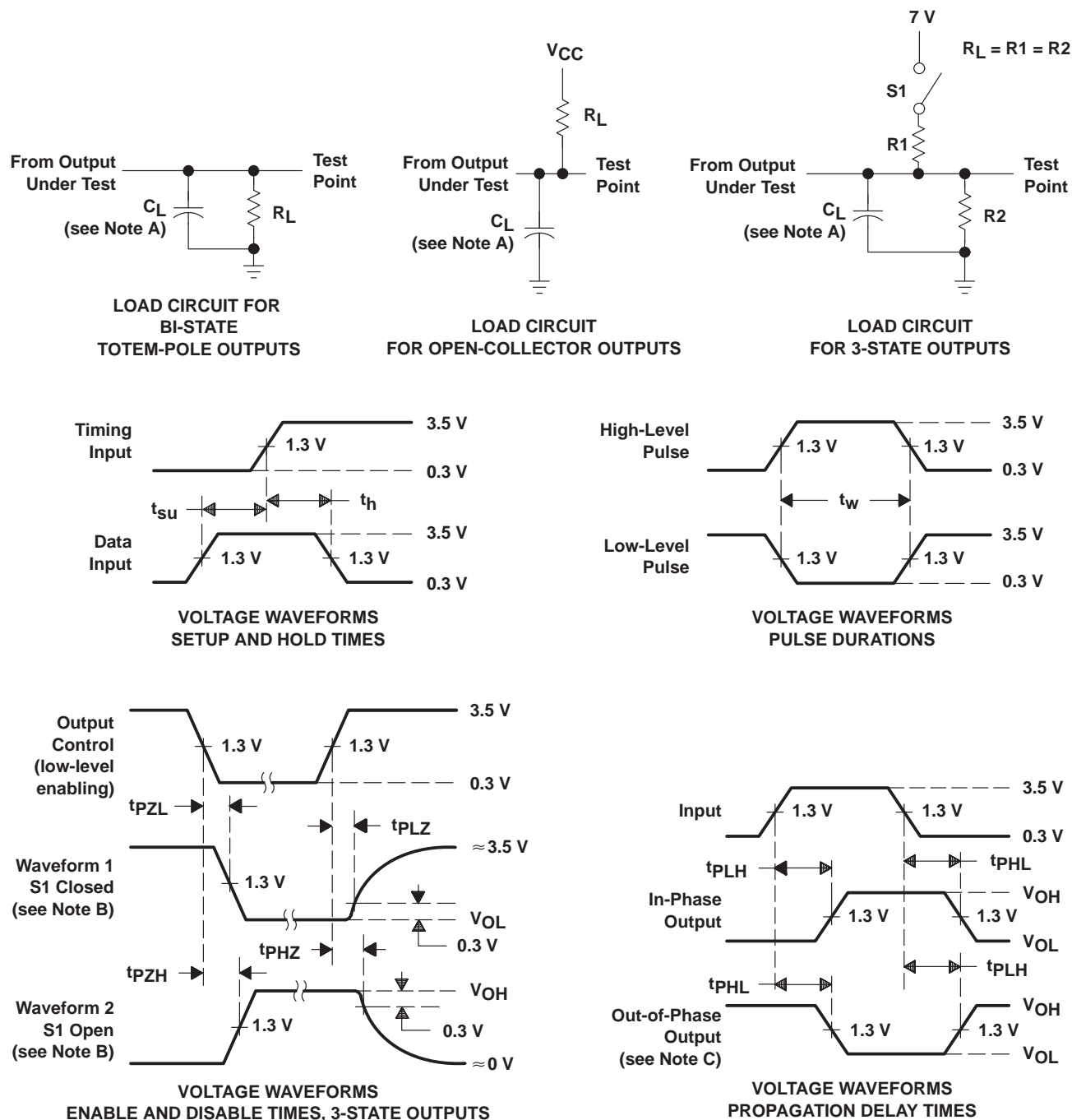
switching characteristics (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§ | | | | UNIT |
|--------------------|-------------------------|-------------------------|---|-----|-----------|-----|------|
| | | | SN54AS869 | | SN74AS869 | | |
| | | | MIN | MAX | MIN | MAX | |
| f _{max} * | | | 40 | | 45 | MHz | |
| t _{PLH} | CLK | $\overline{\text{RCO}}$ | 6 | 35 | 6 | 35 | ns |
| t _{PHL} | | | 6 | 20 | 6 | 18 | |
| t _{PLH} | CLK | Any Q | 3 | 12 | 3 | 11 | ns |
| t _{PHL} | | | 4 | 16 | 4 | 15 | |
| t _{PLH} | $\overline{\text{ENT}}$ | $\overline{\text{RCO}}$ | 3 | 25 | 3 | 15 | ns |
| t _{PHL} | | | 6 | 21 | 6 | 17 | |
| t _{PLH} | $\overline{\text{ENP}}$ | $\overline{\text{RCO}}$ | 5 | 27 | 5 | 19 | ns |
| t _{PHL} | | | 6 | 21 | 6 | 18 | |

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.