

## RTC Module With 32Kx8 NVSRAM

### Features

- Integrated SRAM, real-time clock, crystal, power-fail control circuit, and battery
- Real-Time Clock counts seconds through years in BCD format
- RAM-like clock access
- Pin-compatible with industry-standard 32K x 8 SRAMs
- Unlimited write cycles
- 10-year minimum data retention and clock operation in the absence of power
- Automatic power-fail chip deselect and write-protection
- Software clock calibration for greater than 1 minute per month accuracy
- 10% tolerance of  $V_{CC}$  for write-protect

### General Description

The bq4830Y RTC Module is a non-volatile 262,144-bit SRAM organized as 32,768 words by 8 bits with an integral accessible real-time clock.

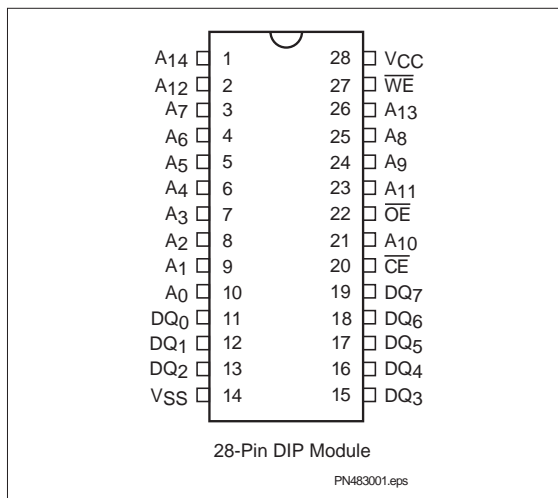
The device combines an internal lithium battery, quartz crystal, clock and power-fail chip, and a full CMOS SRAM in a plastic 28-pin DIP module. The RTC Module directly replaces industry-standard SRAMs and also fits into many EPROM and EEPROM sockets without any requirement for special write timing or limitations on the number of write cycles.

Registers for the real-time clock and clock calibration are located in registers 7FF8h–7FFFh of the memory array.

The clock registers are dual-port read/write SRAM locations that are updated once per second by a clock control circuit from the internal clock counters. The dual-port registers allow clock updates to occur without interrupting normal access to the rest of the SRAM array.

The bq4830Y also contains a power fail-detect circuit. The circuit deselects the device whenever  $V_{CC}$  falls below tolerance, providing a high degree of data security. The battery is electrically isolated when shipped from the factory to provide maximum battery capacity. The battery remains disconnected until the first application of  $V_{CC}$ .

### Pin Connections



### Pin Names

$A_0$ – $A_{14}$	Address input
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
$DQ_0$ – $DQ_7$	Data in/data out
$V_{CC}$	+5 volts
$V_{SS}$	Ground

# bq4830Y

## Functional Description

including memory and clock interface, and data-retention modes.

Figure 1 is a block diagram of the bq4830Y. The following sections describe the bq4830Y functional operation,

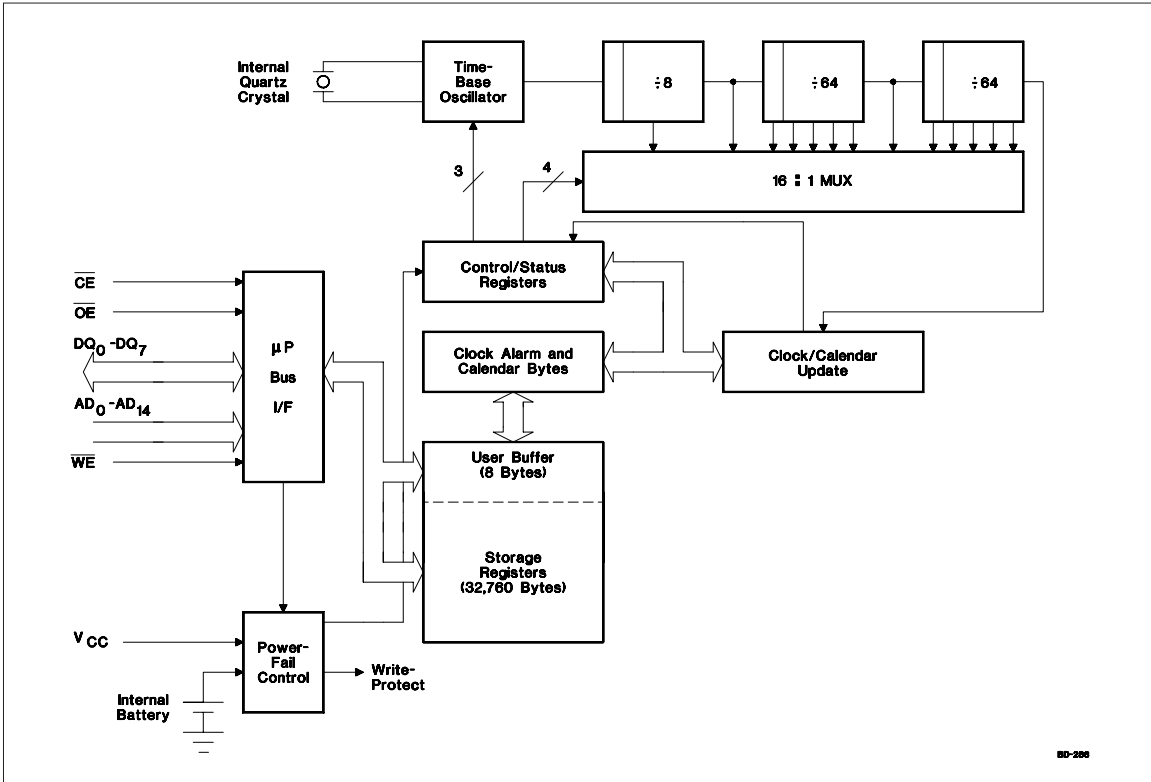


Figure 1. Block Diagram

## Truth Table

V <sub>CC</sub>	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	DQ	Power
< V <sub>CC</sub> (max.)	V <sub>IH</sub>	X	X	Deselect	High Z	Standby
	V <sub>IL</sub>	X	V <sub>IL</sub>	Write	D <sub>IN</sub>	Active
> V <sub>CC</sub> (min.)	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	Read	D <sub>OUT</sub>	Active
	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	Read	High Z	Active
< V <sub>PF<sub>D</sub></sub> (min.) > V <sub>SO</sub>	X	X	X	Deselect	High Z	CMOS standby
≤ V <sub>SO</sub>	X	X	X	Deselect	High Z	Battery-backup mode

Sept. 1996 B

**Address Map**

Figure 2 illustrates the address map for the bq4830Y. Table 1 is a map of the bq4830Y registers.

The bq4830Y provides 8 bytes of clock and control status registers and 32,760 bytes of storage RAM.

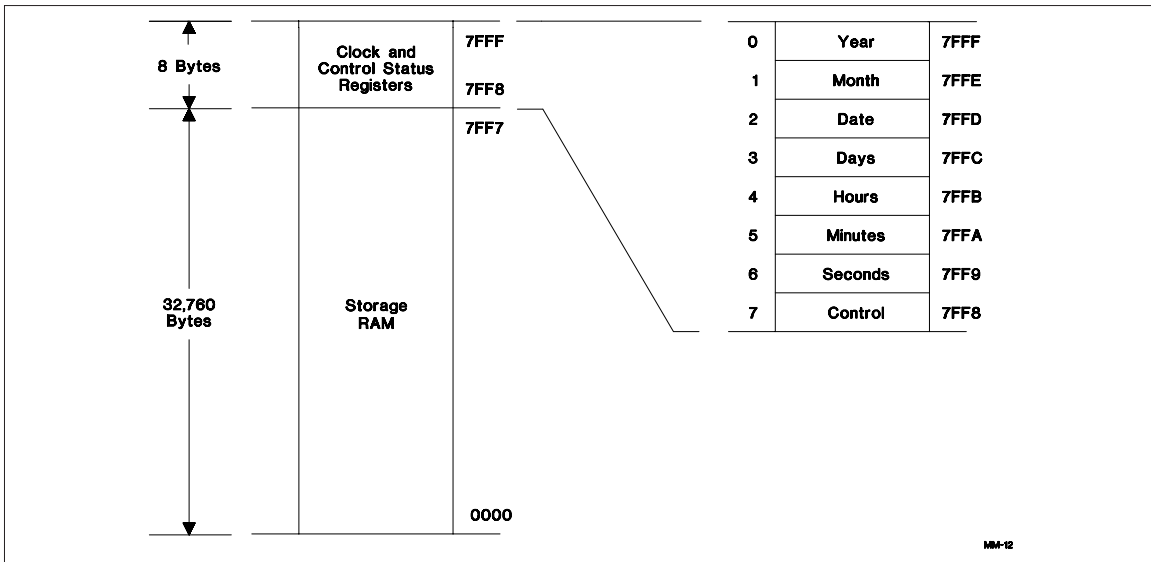


Figure 2. Address Map

Table 1. bq4830Y Clock and Control Register Map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Range (h)	Register
7FFF	10 Years				Year				00-99	Year
7FFE	X	X	X	10 Month	Month				01-12	Month
7FFD	X	X	10 Date		Date				01-31	Date
7FFC	X	FTE	X	X	X	Day			01-07	Days
7FFB	X	X	10 Hours		Hours				00-23	Hours
7FFA	X	10 Minutes			Minutes				00-59	Minutes
7FF9	OSC	10 Seconds			Seconds				00-59	Seconds
7FF8	W	R	S	Calibration				00-31	Control	

**Notes:** X = Unused bits; can be written and read.  
 Clock/Calendar data in 24-hour BCD format.  
 OSC = 1 stops the clock oscillator.

# bq4830Y

---

## Memory Interface

### Read Mode

The bq4830Y is in read mode whenever  $\overline{OE}$  (output enable) is low and  $\overline{CE}$  (chip enable) is low. The device architecture allows ripple-through access of data from eight of 262,144 locations in the static storage array. Thus, the unique address specified by the 15 address inputs defines which one of the 32,768 bytes of data is to be accessed. Valid data is available at the data I/O pins within  $t_{AA}$  (address access time) after the last address input signal is stable, providing that the  $\overline{CE}$  and  $\overline{OE}$  (output enable) access times are also satisfied. If the  $\overline{CE}$  and  $\overline{OE}$  access times are not met, valid data is available after the latter of chip enable access time ( $t_{ACE}$ ) or output enable access time ( $t_{OE}$ ).

$\overline{CE}$  and  $\overline{OE}$  control the state of the eight three-state data I/O signals. If the outputs are activated before  $t_{AA}$ , the data lines are driven to an indeterminate state until  $t_{AA}$ . If the address inputs are changed while  $\overline{CE}$  and  $\overline{OE}$  remain low, output data remains valid for  $t_{OH}$  (output data hold time), but goes indeterminate until the next address access.

### Write Mode

The bq4830Y is in write mode whenever  $\overline{WE}$  and  $\overline{CE}$  are active. The start of a write is referenced from the latter-occurring falling edge of  $\overline{WE}$  or  $\overline{CE}$ . A write is terminated by the earlier rising edge of  $\overline{WE}$  or  $\overline{CE}$ . The addresses must be held valid throughout the cycle.  $\overline{CE}$  or  $\overline{WE}$  must return high for a minimum of  $t_{WR2}$  from  $\overline{CE}$  or  $t_{WR1}$  from  $\overline{WE}$  prior to the initiation of another read or write cycle.

Data-in must be valid  $t_{DW}$  prior to the end of write and remain valid for  $t_{DH1}$  or  $t_{DH2}$  afterward.  $\overline{OE}$  should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on  $\overline{CE}$  and  $\overline{OE}$ , a low on  $\overline{WE}$  disables the outputs  $t_{WZ}$  after  $\overline{WE}$  falls.

### Data-Retention Mode

With valid  $V_{CC}$  applied, the bq4830Y operates as a conventional static RAM. Should the supply voltage decay, the RAM automatically power-fail deselects, write-protecting itself  $t_{WPT}$  after  $V_{CC}$  falls below  $V_{PFD}$ . All outputs become high impedance, and all inputs are treated as "don't care."

If power-fail detection occurs during a valid access, the memory cycle continues to completion. If the memory cycle fails to terminate within time  $t_{WPT}$ , write-protection takes place. When  $V_{CC}$  drops below  $V_{SO}$ , the control circuit switches power to the internal energy source, which preserves data.

The internal coin cell maintains data in the bq4830Y after the initial application of  $V_{CC}$  for an accumulated period of at least 10 years when  $V_{CC}$  is less than  $V_{SO}$ . As system power returns and  $V_{CC}$  rises above  $V_{SO}$ , the battery is disconnected, and the power supply is switched to external  $V_{CC}$ . Write-protection continues for  $t_{CER}$  after  $V_{CC}$  reaches  $V_{PFD}$  to allow for processor stabilization. After  $t_{CER}$ , normal RAM operation can resume.

## Clock Interface

### Reading the Clock

The interface to the clock and control registers of the bq4830Y is the same as that for the general-purpose storage memory. Once every second, the user-accessible clock/calendar locations are updated simultaneously from the internal real time counters. To prevent reading data in transition, updates to the bq4830Y clock registers should be halted. Updating is halted by setting the read bit D6 of the control register to 1. As long as the read bit is 1, updates to user-accessible clock locations are inhibited. Once the frozen clock information is retrieved by reading the appropriate clock memory locations, the read bit should be reset to 0 in order to allow updates to occur from the internal counters. Because the internal counters are not halted by setting the read bit, reading the clock locations has no effect on clock accuracy. Once the read bit is reset to 0, within one second the internal registers update the user-accessible registers with the correct time. A halt command issued during a clock update allows the update to occur before freezing the data.

### Setting the Clock

Bit D7 of the control register is the write bit. Like the read bit, the write bit when set to a 1 halts updates to the clock/calendar memory locations. Once frozen, the locations can be written with the desired information in 24-hour BCD format. Resetting the write bit to 0 causes the written values to be transferred to the internal clock counters and allows updates to the user-accessible registers to resume within one second. Use the write bit, D7, only when updating the time registers (7FFF-7FF9).

### Stopping and Starting the Clock Oscillator

The OSC bit in the seconds register turns the clock on or off. If the bq4830Y is to spend a significant period of time in storage, the clock oscillator can be turned off to preserve battery capacity. OSC set to 1 stops the clock oscillator. When OSC is reset to 0, the clock oscillator is turned on and clock updates to user-accessible memory locations occur within one second.

The OSC bit is set to 1 when shipped from the Benchmark factory.

### Calibrating the Clock

The bq4830Y real-time clock is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The quartz crystal is contained within the bq4830Y package along with the battery. The clock accuracy of the bq4830Y module is tested to be within 20ppm or about 1 minute per month at 25°C. The oscillation rates of crystals change with temperature as Figure 3 shows. To compensate for the frequency shift, the bq4830Y offers onboard software clock calibration. The user can adjust the calibration based on the typical operating temperature of individual applications.

The software calibration bits are located in the control register. Bits D0–D4 control the magnitude of correction, and bit D5 the direction (positive or negative) of correction. Assuming that the oscillator is running at exactly 32,786 Hz, each calibration step of D0–D4 adjusts the clock rate by +4.068 ppm (+10.7 seconds per month) or -2.034 ppm (-5.35 seconds per month) depending on the value of the sign bit D5. When the sign bit is 1, positive adjustment occurs; a 0 activates negative adjustment. The total range of clock calibration is +5.5 or -2.75 minutes per month.

Two methods can be used to ascertain how much calibration a given bq4830Y may require in a system. The first involves simply setting the clock, letting it run for a month, and then comparing the time to an accurate known reference like WWV radio broadcasts. Based on the variation to the standard, the end user can adjust the clock to match the system's environment even after the product is packaged in a non-serviceable enclosure. The only requirement is a utility that allows the end user to access the calibration bits in the control register.

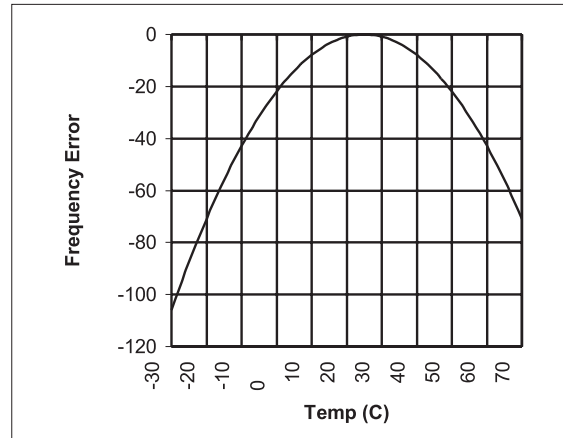


Figure 3. Frequency Error

The second approach uses a bq4830Y test mode. When the frequency test mode enable bit FTE in the days register is set to a 1, and the oscillator is running at exactly 32,768 Hz, the LSB of the seconds register toggles at 512 Hz. Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.01024 Hz indicates a  $(1E6 * 0.01024)/512$  or +20 ppm oscillator frequency error, requiring ten steps of negative calibration ( $10 * -2.034$  or -20.34) or 001010 to be loaded into the calibration byte for correction. To read the test frequency, the bq4830Y must be selected and held in an extended read of the seconds register, location 7FF9, without having the read bit set. The frequency appears on DQ0. The FTE bit must be set using the write bit control. The FTE bit must be reset to 0 for normal clock operation to resume.

## bq4830Y

---

### Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
V <sub>CC</sub>	DC voltage applied on V <sub>CC</sub> relative to V <sub>SS</sub>	-0.3 to 7.0	V	
V <sub>T</sub>	DC voltage applied on any pin excluding V <sub>CC</sub> relative to V <sub>SS</sub>	-0.3 to 7.0	V	V <sub>T</sub> ≤ V <sub>CC</sub> + 0.3
T <sub>OPR</sub>	Operating temperature	0 to +70	°C	
T <sub>STG</sub>	Storage temperature (V <sub>CC</sub> off; oscillator off)	-40 to +70	°C	
T <sub>BIAS</sub>	Temperature under bias	-10 to +70	°C	
T <sub>SOLDER</sub>	Soldering temperature	+260	°C	For 10 seconds

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

### Recommended DC Operating Conditions (T<sub>A</sub> = T<sub>OPR</sub>)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V	
V <sub>SS</sub>	Supply voltage	0	0	0	V	
V <sub>IL</sub>	Input low voltage	-0.3	-	0.8	V	
V <sub>IH</sub>	Input high voltage	2.2	-	V <sub>CC</sub> + 0.3	V	

**Note:** Typical values indicate operation at T<sub>A</sub> = 25°C.

**DC Electrical Characteristics** ( $T_A = T_{OPR}$ ,  $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
$I_{LI}$	Input leakage current	-	-	$\pm 1$	$\mu A$	$V_{IN} = V_{SS}$ to $V_{CC}$
$I_{LO}$	Output leakage current	-	-	$\pm 1$	$\mu A$	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$
$V_{OH}$	Output high voltage	2.4	-	-	V	$I_{OH} = -1.0$ mA
$V_{OL}$	Output low voltage	-	-	0.4	V	$I_{OL} = 2.1$ mA
$I_{SB1}$	Standby supply current	-	3	6	mA	$\overline{CE} = V_{IH}$
$I_{SB2}$	Standby supply current	-	2	4	mA	$\overline{CE} \geq V_{CC} - 0.2V$ , $0V \leq V_{IN} \leq 0.2V$ , or $V_{IN} \geq V_{CC} - 0.2V$
$I_{CC}$	Operating supply current	-	55	75	mA	Min. cycle, duty = 100%, $\overline{CE} = V_{IL}$ , $I_{I/O} = 0$ mA
$V_{PFD}$	Power-fail-detect voltage	4.30	4.37	4.50	V	
$V_{SO}$	Supply switch-over voltage	-	3	-	V	

**Notes:** Typical values indicate operation at  $T_A = 25^\circ C$ ,  $V_{CC} = 5V$ .

**Capacitance** ( $T_A = 25^\circ C$ ,  $F = 1MHz$ ,  $V_{CC} = 5.0V$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$C_{I/O}$	Input/output capacitance	-	-	10	pF	Output voltage = 0V
$C_{IN}$	Input capacitance	-	-	10	pF	Input voltage = 0V

**Note:** These parameters are sampled and not 100% tested.

# bq4830Y

## AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5 ns
Input and output timing reference levels	1.5 V (unless otherwise specified)
Output load (including scope and jig)	See Figures 4 and 5

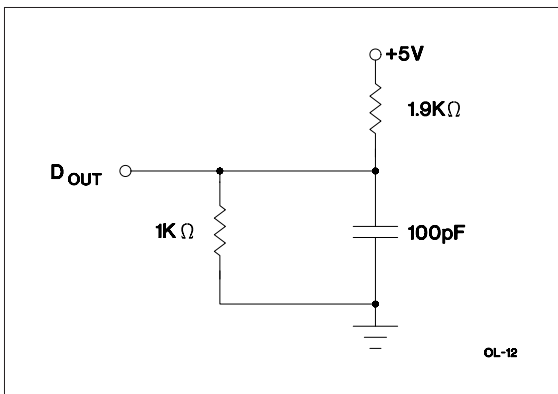


Figure 4. Output Load A

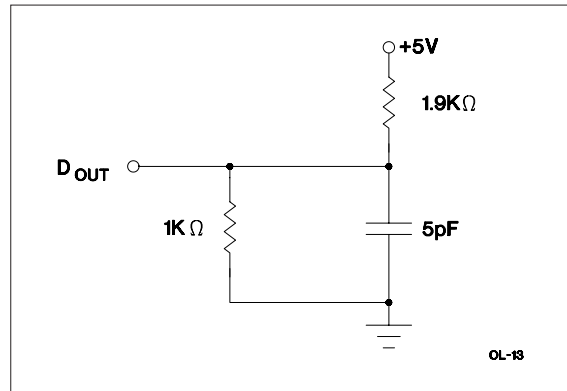


Figure 5. Output Load B

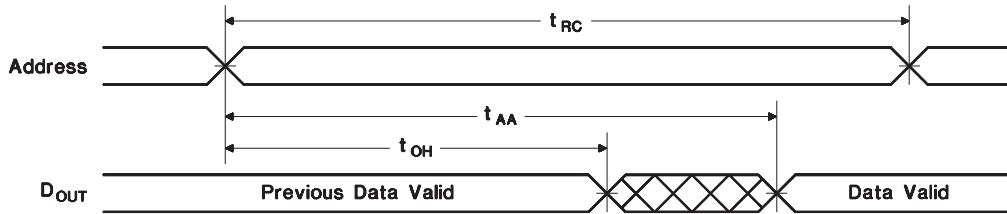
## Read Cycle ( $T_A = T_{OPR}$ , $V_{CCmin} \leq V_{CC} \leq V_{CCmax}$ )

Symbol	Parameter	-85		Unit	Conditions
		Min.	Max.		
t <sub>RC</sub>	Read cycle time	85	-	ns	
t <sub>AA</sub>	Address access time	-	85	ns	Output load A
t <sub>ACE</sub>	Chip enable access time	-	85	ns	Output load A
t <sub>OE</sub>	Output enable to output valid	-	45	ns	Output load A
t <sub>CLZ</sub>	Chip enable to output in low Z	5	-	ns	Output load B
t <sub>OLZ</sub>	Output enable to output in low Z	0	-	ns	Output load B
t <sub>CHZ</sub>	Chip disable to output in high Z	0	35	ns	Output load B
t <sub>OHZ</sub>	Output disable to output in high Z	0	25	ns	Output load B
t <sub>OH</sub>	Output hold from address change	10	-	ns	Output load A

Sept. 1996 B

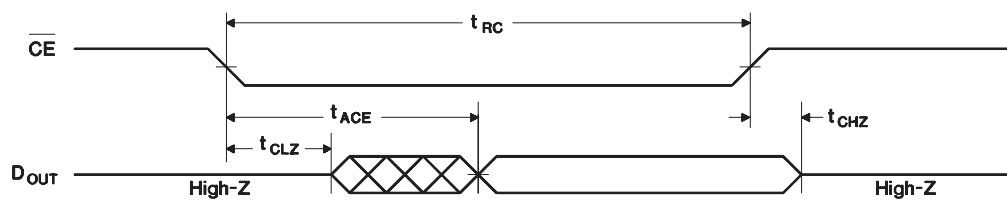


Read Cycle number 1 (Address Access) <sup>1,2</sup>



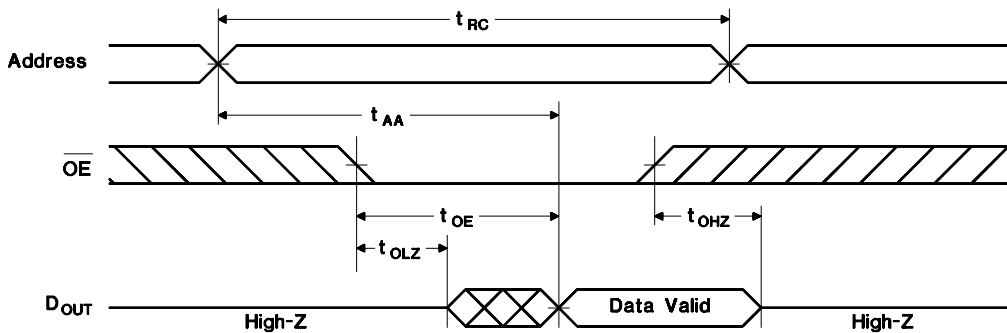
Read Cycle number 2 ( $\overline{CE}$  Access) <sup>1,3,4</sup>

RC-1



RC-2

Read Cycle No. 3 (OE Access) <sup>1,5</sup>



RC-3

- Notes:**
1.  $\overline{WE}$  is held high for a read cycle..
  2. Device is continuously selected:  $\overline{CE} = \overline{OE} = V_{IL}$ .
  3. Address is valid prior to or coincident with  $\overline{CE}$  transition low.
  4.  $\overline{OE} = V_{IL}$ .
  5. Device is continuously selected:  $\overline{CE} = V_{IL}$ .

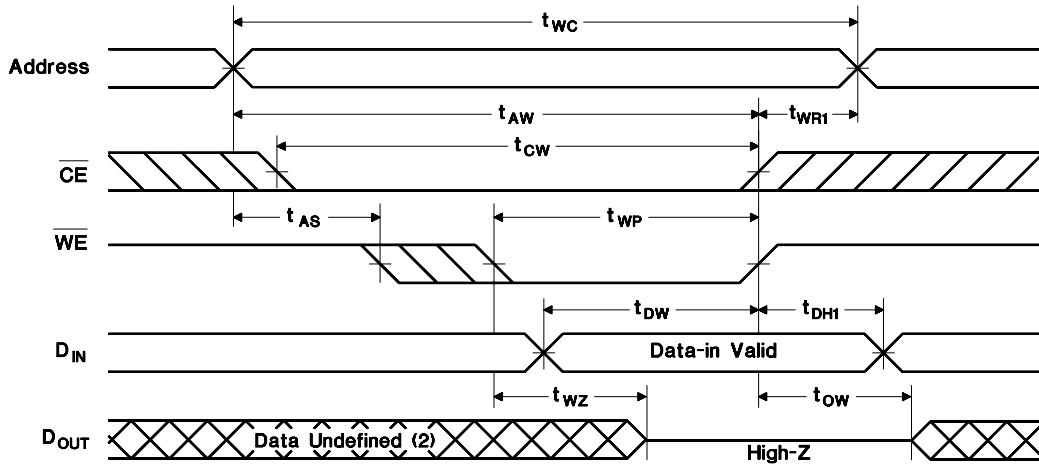
## bq4830Y

### Write Cycle ( $T_A = T_{OPR}$ , $V_{CCMIN} \leq V_{CC} \leq V_{CCMAX}$ )

Symbol	Parameter	-85		Units	Conditions/Notes
		Min.	Max.		
t <sub>WC</sub>	Write cycle time	85	-	ns	
t <sub>CW</sub>	Chip enable to end of write	75	-	ns	(1)
t <sub>AW</sub>	Address valid to end of write	75	-	ns	(1)
t <sub>AS</sub>	Address setup time	0	-	ns	Measured from address valid to beginning of write. (2)
t <sub>WP</sub>	Write pulse width	65	-	ns	Measured from beginning of write to end of write. (1)
t <sub>WR1</sub>	Write recovery time (write cycle 1)	5	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (3)
t <sub>WR2</sub>	Write recovery time (write cycle 2)	15	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (3)
t <sub>DW</sub>	Data valid to end of write	35	-	ns	Measured to first low-to-high transition of either $\overline{CE}$ or $\overline{WE}$ .
t <sub>DH1</sub>	Data hold time (write cycle 1)	0	-	ns	Measured from $\overline{WE}$ going high to end of write cycle. (4)
t <sub>DH2</sub>	Data hold time (write cycle 2)	10	-	ns	Measured from $\overline{CE}$ going high to end of write cycle. (4)
t <sub>WZ</sub>	Write enabled to output in high Z	0	30	ns	I/O pins are in output state. (5)
t <sub>OW</sub>	Output active from end of write	0	-	ns	I/O pins are in output state. (5)

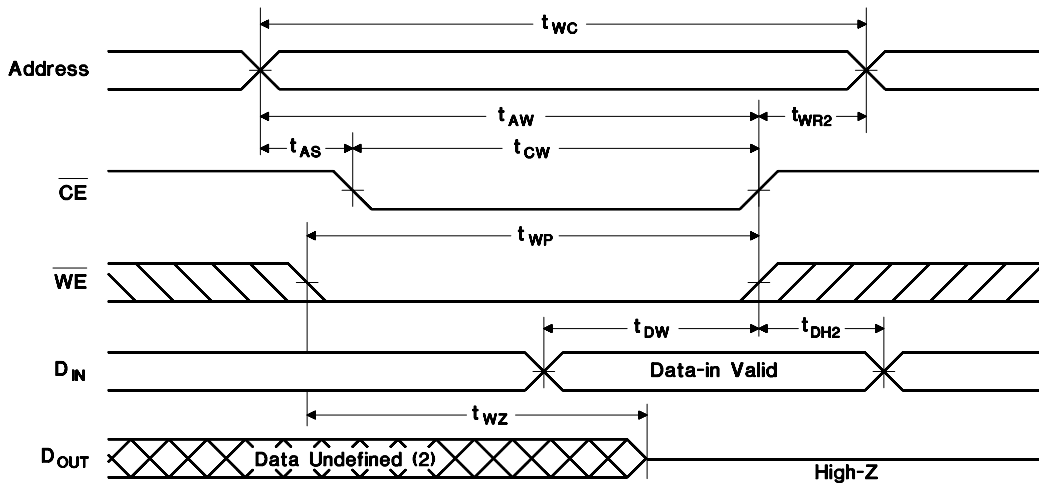
- Notes:**
1. A write ends at the earlier transition of  $\overline{CE}$  going high and  $\overline{WE}$  going high.
  2. A write occurs during the overlap of a low  $\overline{CE}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CE}$  going low and  $\overline{WE}$  going low.
  3. Either t<sub>WR1</sub> or t<sub>WR2</sub> must be met.
  4. Either t<sub>DH1</sub> or t<sub>DH2</sub> must be met.
  5. If  $\overline{CE}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in high-impedance state.

**Write Cycle No. 1 (WE-Controlled)** <sup>1,2,3</sup>



WC-14

**Write Cycle No. 2 (CE-Controlled)** <sup>1,2,3,4,5</sup>



WC-15

- Notes:**
1.  $\overline{CE}$  or  $\overline{WE}$  must be high during address transition.
  2. Because I/O may be active ( $\overline{OE}$  low) during this period, data input signals of opposite polarity to the outputs must not be applied.
  3. If  $\overline{OE}$  is high, the I/O pins remain in a state of high impedance.
  4. Either  $t_{WR1}$  or  $t_{WR2}$  must be met.
  5. Either  $t_{DH1}$  or  $t_{DH2}$  must be met.

# bq4830Y

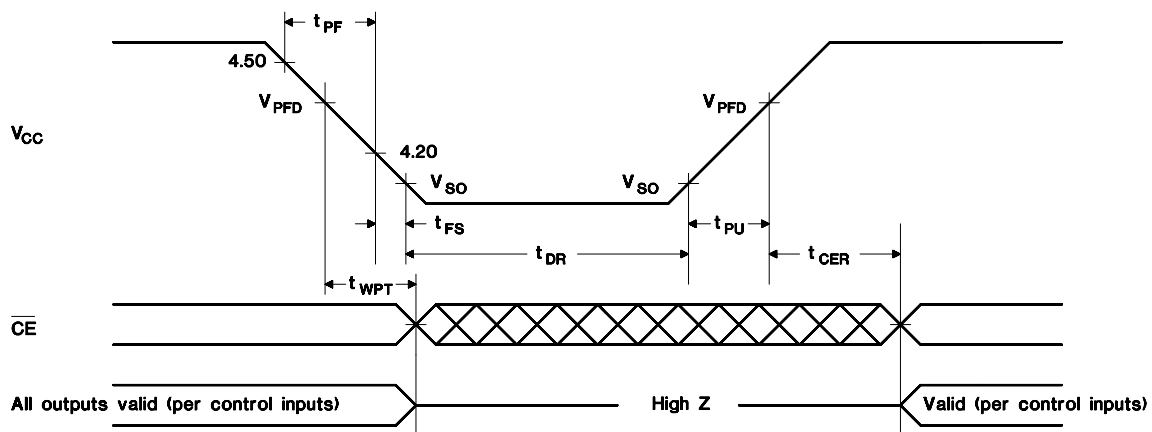
## Power-Down/Power-Up Cycle ( $T_A = T_{OPR}$ )

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
$t_{PF}$	$V_{CC}$ slew, 4.50 to 4.20 V	300	-	-	$\mu\text{s}$	
$t_{FS}$	$V_{CC}$ slew, 4.20 to $V_{SO}$	10	-	-	$\mu\text{s}$	
$t_{PU}$	$V_{CC}$ slew, $V_{SO}$ to $V_{PFD}$ (max.)	0	-	-	$\mu\text{s}$	
$t_{CER}$	Chip enable recovery time	40	100	200	ms	Time during which SRAM is write-protected after $V_{CC}$ passes $V_{PFD}$ on power-up.
$t_{DR}$	Data-retention time in absence of $V_{CC}$	10	-	-	years	$T_A = 25^\circ\text{C}$ . (2)
$t_{WPT}$	Write-protect time	40	100	160	$\mu\text{s}$	Delay after $V_{CC}$ slews down past $V_{PFD}$ before SRAM is write-protected.

- Notes:**
1. Typical values indicate operation at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ .
  2. Battery is disconnected from circuit until after  $V_{CC}$  is applied for the first time.  $t_{DR}$  is the accumulated time in absence of power beginning when power is first applied to the device.

**Caution:** Negative undershoots below the absolute maximum rating of  $-0.3\text{V}$  in battery-backup mode may affect data integrity.

## Power-Down/Power-Up Timing



PD-16

Sept. 1996 B

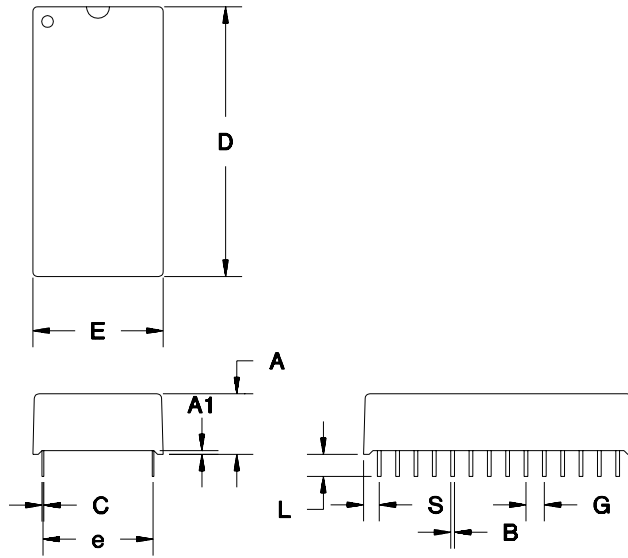
### Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	7	Value change	I <sub>SB1</sub> and max. were 4, 7; are now 3, 6
1	7	Value change	I <sub>SB2</sub> typ. was 2.5; is now 2

**Note:** Change 1 = Sept. 1996 B changes from Oct. 1995.

# bq4830Y

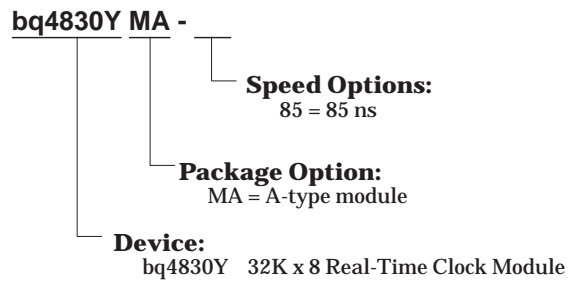
## MA: 28-Pin A-Type Module



28-Pin MA (A-Type Module)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.365	0.375	9.27	9.53
A1	0.015	-	0.38	-
B	0.017	0.023	0.43	0.58
C	0.008	0.013	0.20	0.33
D	1.470	1.500	37.34	38.10
E	0.710	0.740	18.03	18.80
e	0.590	0.630	14.99	16.00
G	0.090	0.110	2.29	2.79
L	0.120	0.150	3.05	3.81
S	0.075	0.110	1.91	2.79

## Ordering Information



**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
BQ4830YMA-85	ACTIVE			0	1	None	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

This datasheet has been download from:

[www.datasheetcatalog.com](http://www.datasheetcatalog.com)

Datasheets for electronics components.