

# DATA SHEET

**TDA2613**

**6 W hi-fi audio power amplifier**

Product specification  
File under Integrated circuits, IC01

July 1994

**6 W hi-fi audio power amplifier****TDA2613****GENERAL DESCRIPTION**

The TDA2613 is a hi-fi audio power amplifier encapsulated in a 9-lead SIL plastic power package. The device is especially designed for mains fed applications (e.g. tv and radio).

**Features**

- Requires very few external components
- Input muted during power-on and off (no switch-on or switch-off clicks)
- Low offset voltage between output and ground
- Hi-fi according to IEC 268 and DIN 45500
- Short-circuit-proof
- Thermally protected.

**QUICK REFERENCE DATA**

Supply voltage range	$V_P$		15 to 42 V
Output power at THD = 0,5%, $V_P = 24$ V	$P_o$	typ.	6 W
Voltage gain	$G_v$	typ.	30 dB
Supply voltage ripple rejection	SVRR	typ.	60 dB
Noise output voltage	$V_{no(rms)}$	typ.	70 $\mu$ V

**PACKAGE OUTLINE**

TDA2613: 9-lead SIL; plastic power (SOT110B); SOT110-1; 1996 August 07.

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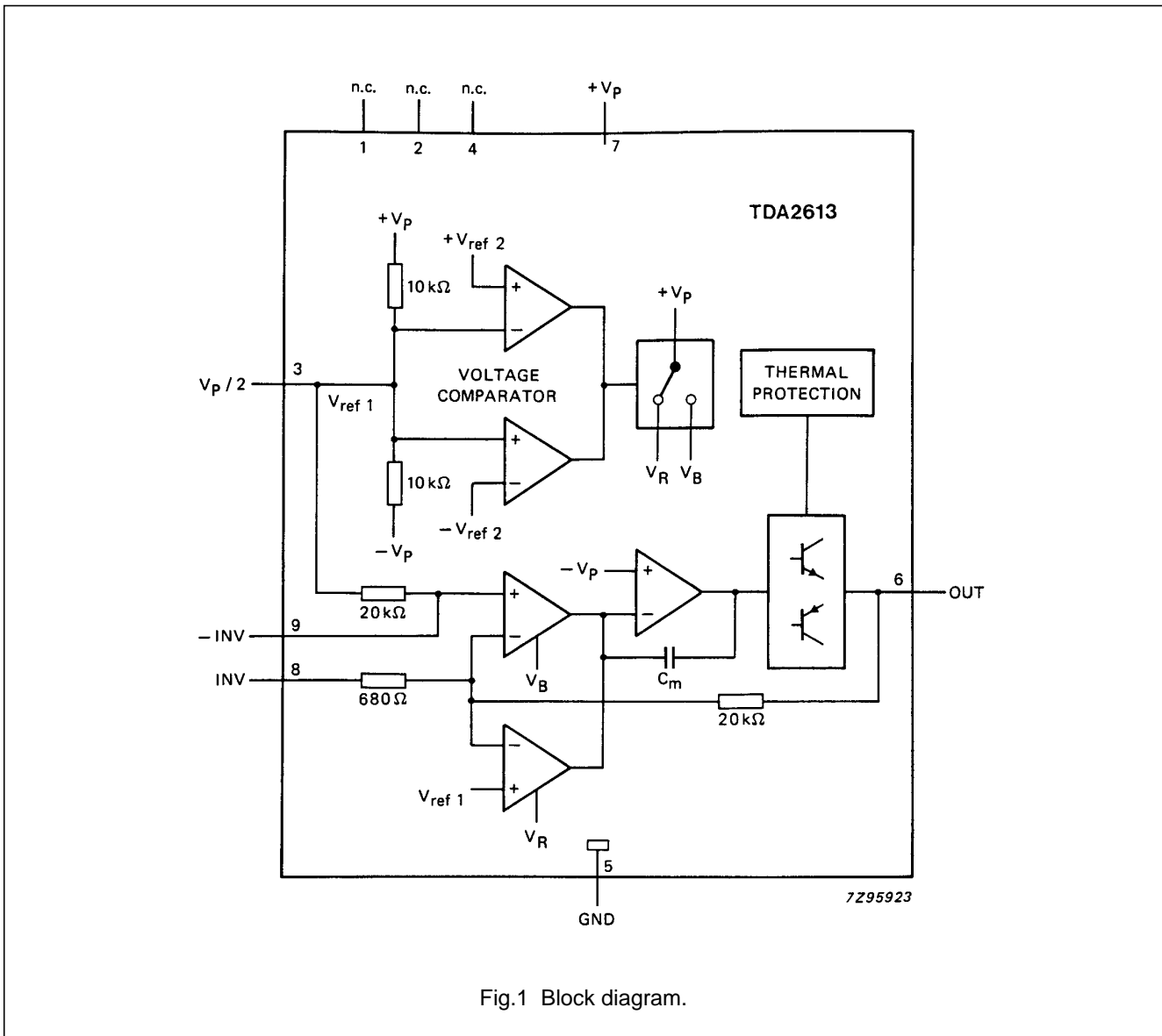


Fig.1 Block diagram.

**PINNING**

1.	n.c.	not connected	5.	GND	ground (asymmetrical) or negative supply (symmetrical)
2.	n.c.	not connected	6.	OUT	output
3.	$V_p/2$	$\frac{1}{2} V_p$ (asymmetrical) or ground (symmetrical)	7.	+V <sub>P</sub>	positive supply
4.	n.c.	not connected	8.	INV	inverting input
			9.	-INV	non-inverting input

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**FUNCTIONAL DESCRIPTION**

This hi-fi power amplifier is designed for mains fed applications. The device is intended for asymmetrical power supplies, but a symmetrical supply may also be used. An output power of 6 watts (THD = 0,5%) can be delivered into an 8  $\Omega$  load with an asymmetrical power supply of 24 V.

The gain is fixed internally at 30 dB. Internal gain fixing gives low gain spread.

A special feature of this device is a mute circuit which suppresses unwanted input signals during switching on and off. Referring to Fig.4, the 100  $\mu$ F capacitor creates a time delay when the voltage at pin 3 is lower than an internally fixed reference voltage. During the delay the amplifier remains in the DC operating mode but is isolated from the non-inverting input on pin 9.

Two thermal protection circuits are provided, one monitors the average junction temperature and the other the instantaneous temperature of the power transistors. Both protection circuits activate at 150  $^{\circ}$ C allowing safe operation to a maximum junction temperature of 150  $^{\circ}$ C without added distortion.

**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

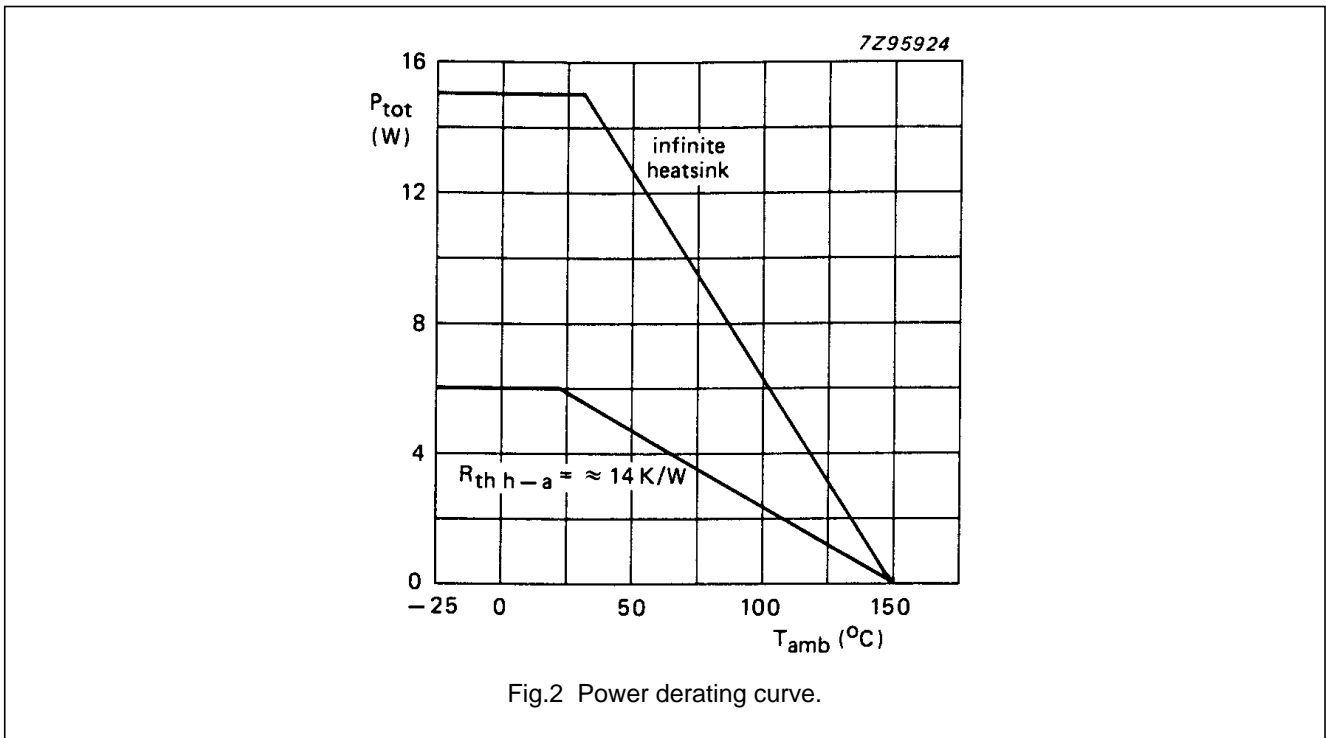
PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Supply voltage		$V_P$	–	42	V
Non-repetitive peak output current		$I_{OSM}$	–	4	A
Total power dissipation	see Fig.2	$P_{tot}$			
Storage temperature range		$T_{stg}$	–55	+ 150	$^{\circ}$ C
Junction temperature		$T_j$	–	150	$^{\circ}$ C
Short-circuit time: outputs short-circuited to ground (full signal drive)	see note	$t_{sc}$	–	1	hour

**Note to the Ratings**

For asymmetrical power supplies (at short-circuiting of the load) the maximum supply voltage is limited to  $V_P = 28$  V. If the total internal resistance of the supply ( $R_S$ )  $\geq 4$   $\Omega$ , the maximum unloaded supply voltage is increased to 32 V. For symmetrical power supplies the circuit is short-circuit proof to  $V_P = \pm 21$  V.

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**THERMAL RESISTANCE**

From junction to case

$$R_{th\ j-c} = 8\ K/W$$

**HEATSINK DESIGN EXAMPLE**

With derating of 8 K/W, the value of heatsink thermal resistance is calculated as follows: given  $R_L = 8\ \Omega$  and  $V_P = 24\ V$ , the measured maximum dissipation is 4,1 W; then, for a maximum ambient temperature of 60 °C, the required thermal resistance of the heatsink is:

$$R_{th\ h-a} = \frac{150 - 60}{4,1} - 8 \approx 14\ K/W$$

Note: The metal tab (heatsink) has the same potential as pin 5 (GND).

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## CHARACTERISTICS

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage range						
operating mode		$V_P$	15	24	42	V
input mute mode		$V_P$	4	–	10	V
Repetitive peak						
output current		$I_{ORM}$	2.2	–	–	A
<b>Operating mode:</b> asymmetrical power supply; test circuit as per Fig.4; $V_P = 24\text{ V}$ ; $R_L = 8\ \Omega$ ; $T_{amb} = 25\text{ }^\circ\text{C}$ ; $f = 1\text{ kHz}$						
Total quiescent current		$I_{tot}$	10	20	35	mA
Output power	THD = 0,5%	$P_o$	5	6	–	W
	THD = 10%	$P_o$	6,5	8,0	–	W
Total harmonic						
distortion	$P_o = 4\text{ W}$	THD	–	0,15	0,2	%
Power bandwidth	THD = 0,5%; note 1	B	–	20 to 16 k	–	Hz
Voltage gain		$G_v$	29	30	31	dB
Noise output voltage						
(r.m.s. value);						
unweighted (20 Hz						
to 20 kHz)	$R_S = 2\text{ k}\Omega$	$V_{no(rms)}$	–	70	140	$\mu\text{V}$
Input impedance		$ Z_i $	14	20	26	$\text{k}\Omega$
Supply voltage						
ripple rejection	note 2	SVRR	35	44	–	dB
Input bias current		$I_{ib}$	–	0,3	–	$\mu\text{A}$
DC output offset						
voltage	with respect to $V_P/2$	$V_{os}$	–	30	200	mV
<b>Input mute mode:</b> asymmetrical power supply; test circuit as per Fig.4; $V_P = 8\text{ V}$ ; $R_L = 8\ \Omega$ ; $T_{amb} = 25\text{ }^\circ\text{C}$ ; $f = 1\text{ kHz}$						
Total quiescent current		$I_{tot}$	5	15	20	mA
Output voltage	$V_i = 600\text{ mV}$	$V_{out}$	–	2,0	2,8	mV
Noise output voltage						
(r.m.s. value);						
unweighted (20 Hz						
to 20 kHz)	$R_S = 2\text{ k}\Omega$	$V_{no(rms)}$	–	70	140	$\mu\text{V}$
Supply voltage						
ripple rejection	note 2	SVRR	35	55	–	dB
DC output offset						
voltage	with respect to $V_P/2$	$V_{os}$	–	40	200	mV

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PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
<b>Operating mode:</b> symmetrical power supply; test circuit as per Fig.3;						
$V_P = \pm 12\text{ V}$ ; $R_L = 8\ \Omega$ ; $T_{\text{amb}} = 25\ \text{°C}$ ; $f = 1\ \text{kHz}$						
Total quiescent current		$I_{\text{tot}}$	10	20	35	mA
Output power	THD = 0,5%	$P_o$	5	6	–	W
	THD = 10%	$P_o$	6,5	8,5	–	W
Total harmonic distortion	$P_o = 4\ \text{W}$	THD	–	0,13	0,2	%
Power bandwidth	THD = 0,5%					
	note 1	B	–	40 to 16 k	–	Hz
Voltage gain		$G_v$	29	30	31	dB
Noise output voltage (r.m.s. value); unweighted (20 Hz to 20 kHz)						
	$R_S = 2\ \text{k}\Omega$	$V_{\text{no(rms)}}$	–	70	140	$\mu\text{V}$
Input impedance		$ Z_i $	14	20	26	$\text{k}\Omega$
Supply voltage ripple rejection		SVRR	40	60	–	dB
DC output offset voltage	with respect to ground	$V_{\text{os}}$	–	30	200	mV

**Notes to the characteristics**

1. Power bandwidth at  $P_{o\ \text{max}} -3\ \text{dB}$ .
2. Ripple rejection at  $R_S = 0\ \Omega$ ,  $f = 100\ \text{Hz}$  to  $20\ \text{kHz}$ ;  
ripple voltage =  $200\ \text{mV}$  (r.m.s. value) applied to positive or negative supply rail.

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APPLICATION INFORMATION

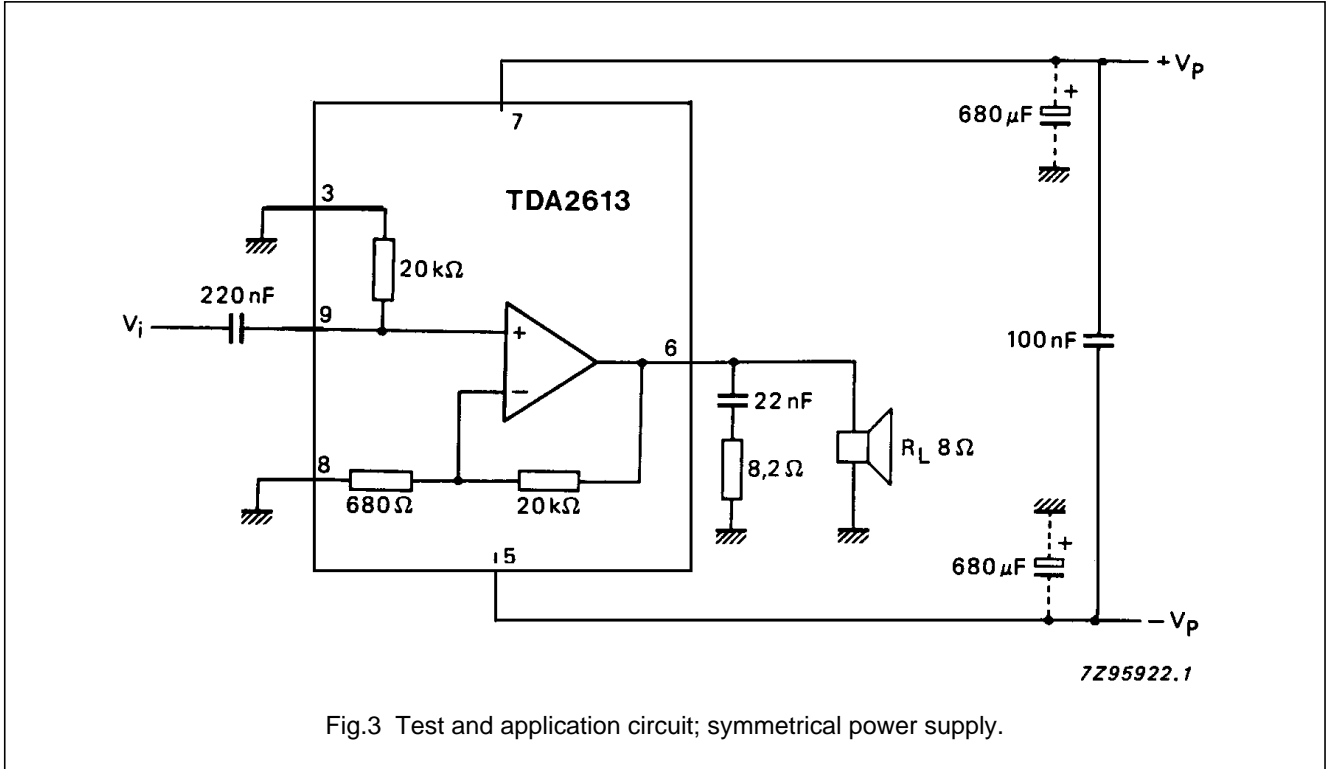


Fig.3 Test and application circuit; symmetrical power supply.

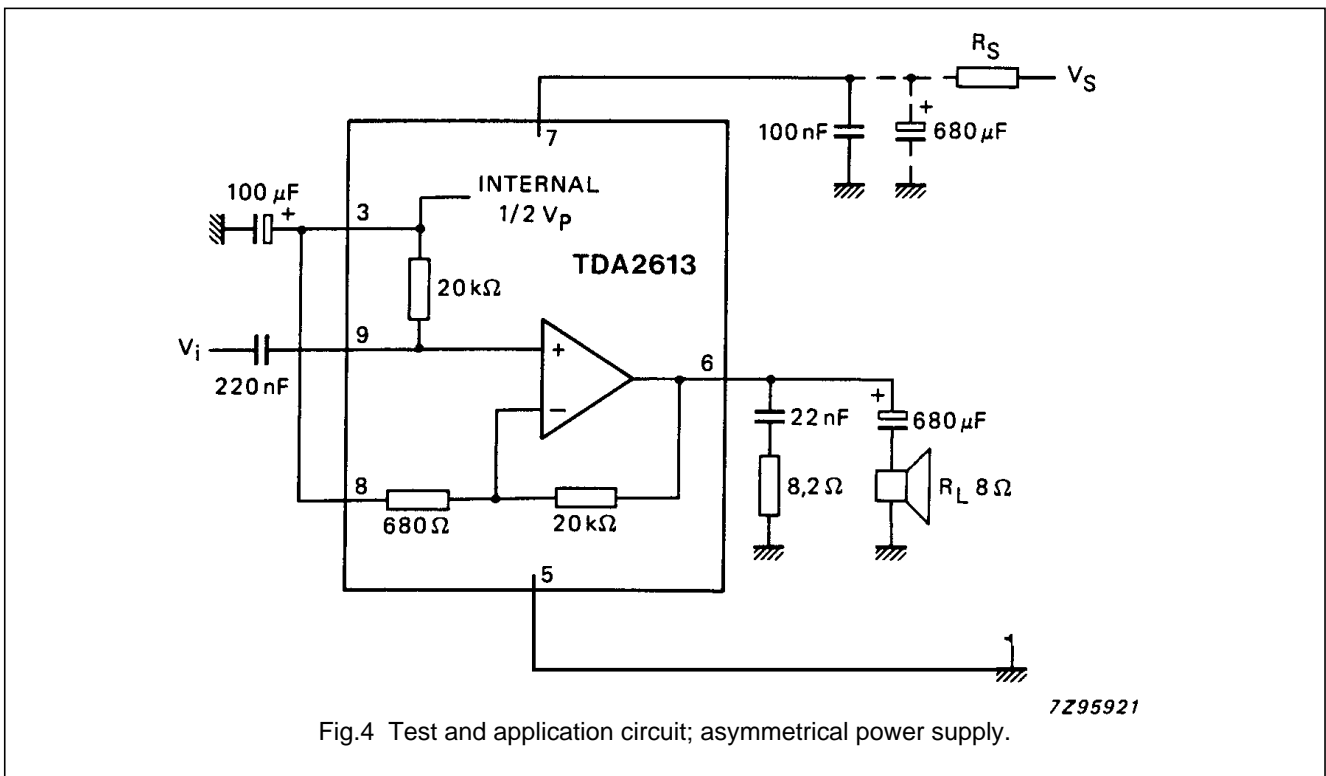


Fig.4 Test and application circuit; asymmetrical power supply.



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**Input mute circuit**

The input mute circuit operates only during switching on and off of the supply voltage. The circuit compares the  $\frac{1}{2}$  supply voltage (at pin 3) with an internally fixed reference voltage ( $V_{ref}$ ), derived directly from the supply voltage. When the voltage at pin 3 is lower than  $V_{ref}$  the non-inverting input (pin 9) is disconnected from the amplifier. The voltage at pin 3 is determined by an internal voltage divider and the external 100  $\mu$ F capacitor.

During switching on, a time delay is created between the reference voltage and the voltage at pin 3, during which the input terminal is disconnected, (as illustrated in Fig.5).

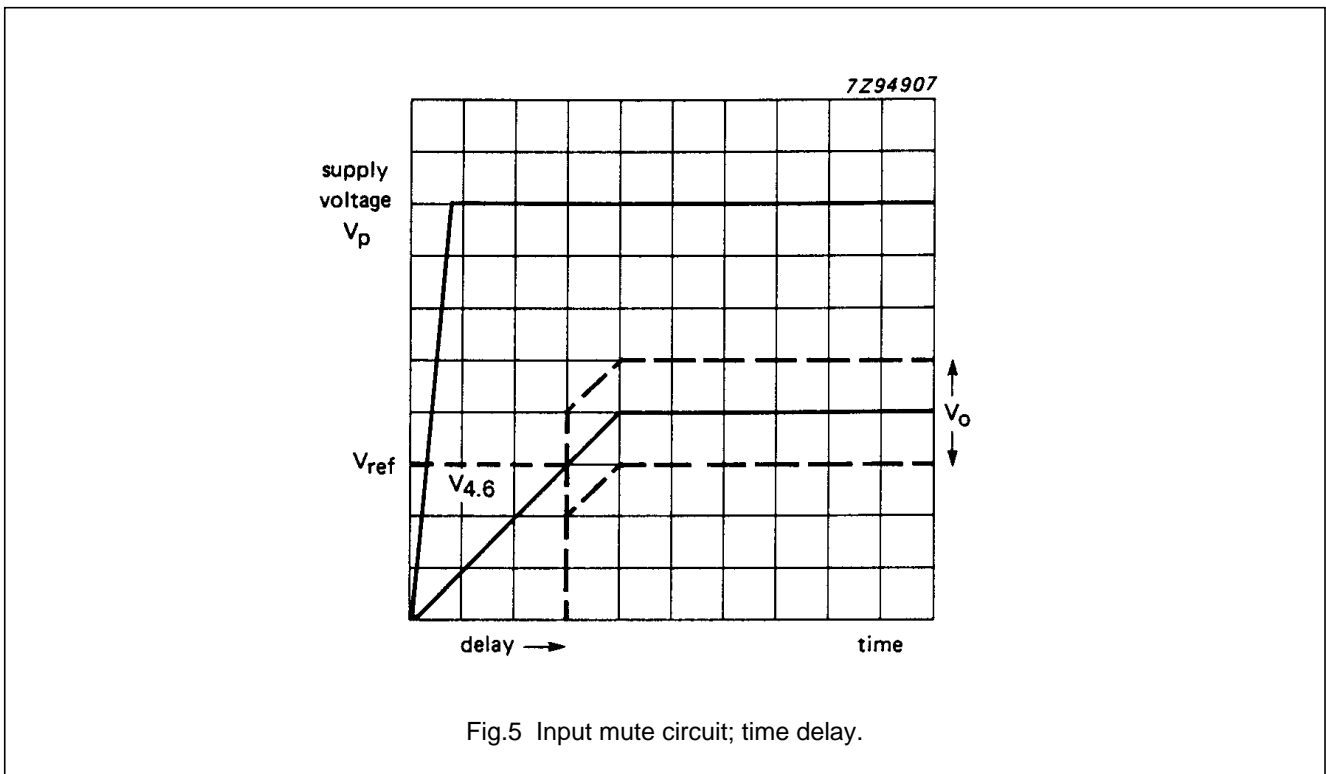


Fig.5 Input mute circuit; time delay.

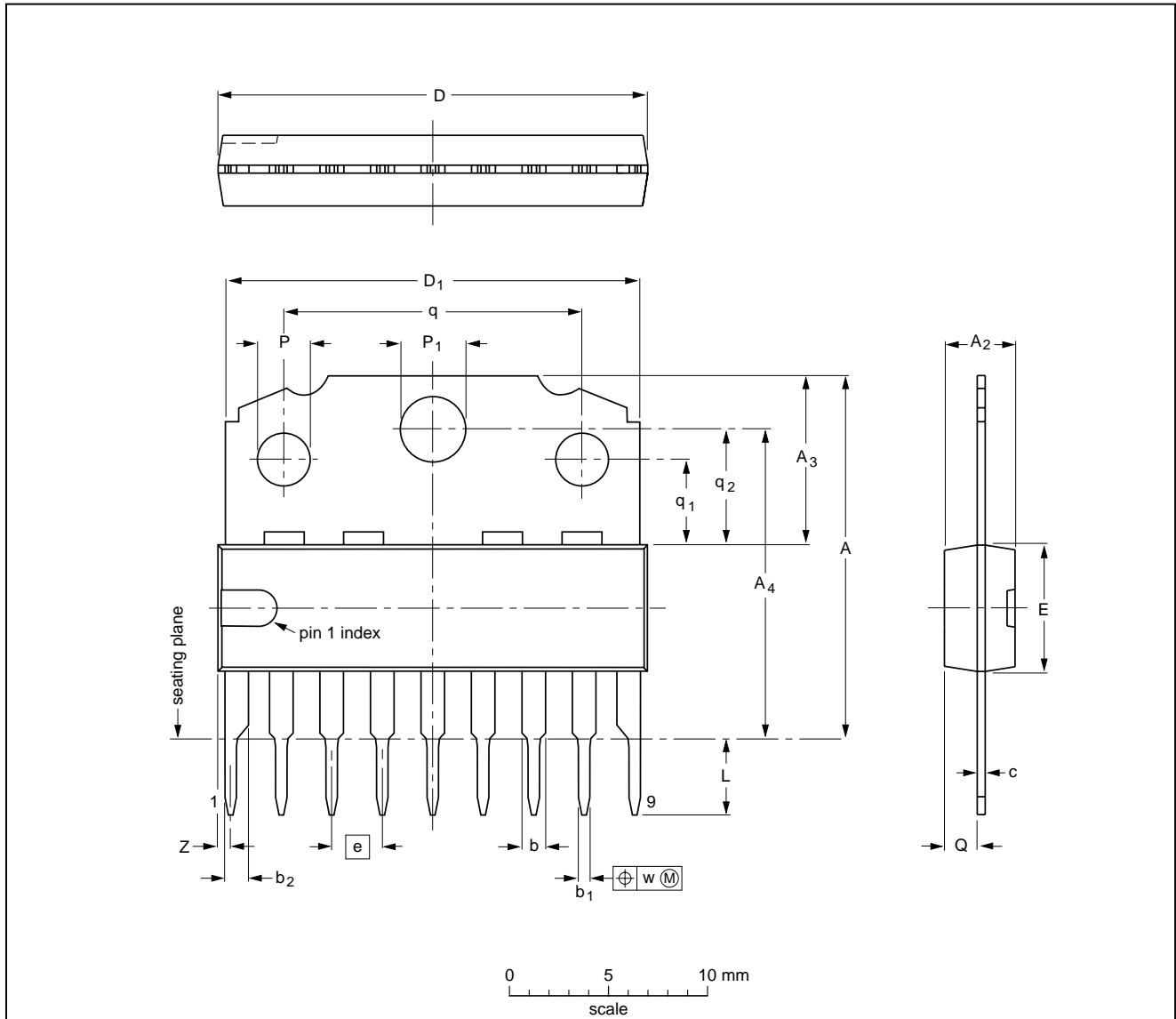
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PACKAGE OUTLINE

SIL9MPF: plastic single in-line medium power package with fin; 9 leads

SOT110-1



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>2</sub> max.	A <sub>3</sub>	A <sub>4</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	D <sub>1</sub>	E <sup>(1)</sup>	e	L	P	P <sub>1</sub>	Q	q	q <sub>1</sub>	q <sub>2</sub>	w	Z <sup>(1)</sup> max.
mm	18.5 17.8	3.7	8.7 8.0	15.8 15.4	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT110-1						92-11-17 95-02-25

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**SOLDERING****Introduction**

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

**Soldering by dipping or by wave**

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

**Repairing soldered joints**

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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