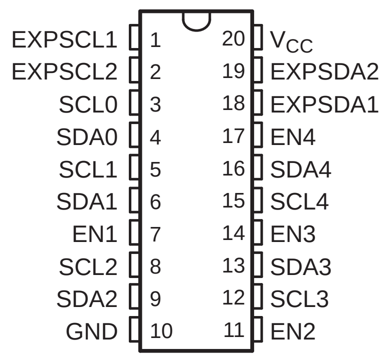
FEATURES

- **Expandable Five-Channel Bidirectional Buffer**
- **400-kHz Fast I^{2}C Bus**
- **Operating V_{CC} Range of 3 V to 3.6 V**
- **5-V Tolerant I^{2}C and Enable Input Pins to Support Mixed-Mode Signal Operation**
- **Active-High Individual Repeater Enable Inputs**
- **Open-Drain Input/Outputs**
- **Lockup-Free Operation**
- **Supports Arbitration and Clock Stretching Across the Repeater**
- **Supports Multiple Masters**
- **Powered-Off High-Impedance I^{2}C Pins**
- **I^{2}C Bus and SMBus Compatible**
- **Latchup Performance Exceeds 100 mA Per JESD 78**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DBQ, DW, OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The PCA9518 is an expandable five-channel bidirectional buffer for I^{2}C and SMBus applications. The I^{2}C protocol requires a maximum bus capacitance of 400 pF, which is derived from the number of devices on the I^{2}C bus and the bus length. The PCA9518 overcomes this restriction by separating and buffering the I^{2}C data (SDA) and clock (SCL) lines into multiple groups of 400-pF segments. Any segment-to-segment transition sees only one repeater delay. Each PCA9518 can communicate with other PCA9518 hubs through a 4-wire inter-hub expansion bus. Using multiple PCA9518 parts, any width hub (in multiples of five) can be implemented using the expansion pins, with only one repeater delay and no functional degradation of the system performance.

ORDERING INFORMATION

T_A	PACKAGE (1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DB	Reel of 2000	PCA9518DBR	PD518
	QSOP – DBQ	Reel of 2500	PCA9518DBQR	PCA9518
	SOIC – DW	Tube of 25	PCA9518DW	PCA9518
		Reel of 2000	PCA9518DWR	
	TSSOP – PW	Tube of 70	PCA9518PW	PD518
		Reel of 2000	PCA9518PWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

DESCRIPTION (CONTINUED)

The device is designed for 3-V to 3.6-V V_{CC} operation, but it has 5-V tolerant I^2C and enable (EN) input pins. This feature allows for translation from 3 V to 5 V between a master and slave. The enable pin also can be used to electrically isolate a repeater segment from the I^2C bus. This is useful in cases where one segment needs to run at 100 kHz while the rest of the system is at 400 kHz. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz, because of the delays added by the repeater.

The output low levels for each internal buffer are approximately 0.5 V, but the input voltage of each internal buffer must be 70 mV or more below the output low level, when the output internally is driven low. This prevents a lockup condition from occurring when the input low condition is released.

A PCA9518 cluster cannot be put in series with a repeater such as the PCA9515 or another PCA9518 cluster, as the design does not allow this configuration. Multiple PCA9518 devices can be grouped with other PCA9518 devices into any size cluster using the EXPxxxx pins that allow the I^2C signals to be sent or received from one PCA9518 to another PCA9518 within the cluster. Because there is no direction pin, slightly different valid low voltage levels are used to avoid lockup conditions between the input and the output of individual repeaters in the cluster. A valid low applied at the input of any of the PCA9518 devices is propagated as a buffered low, with a slightly higher value, to all enabled outputs in the PCA9518 cluster. When this buffered low is applied to another repeater or separate PCA9518 cluster (not connected via the EXPxxxx pins) in series, the second repeater or PCA9518 cluster does not recognize it as a regular low and does not propagate it as a buffered low again. For this reason, the PCA9518 should not be put in series with other repeater or PCA9518 clusters.

The PCA9518 has five multidirectional open-drain buffers designed to support the standard low-level-contention arbitration of the I^2C bus. Except during arbitration or clock stretching, the PCA9518 acts like a pair of noninverting open-drain buffers, one for SDA and one for SCL.

There is an internal power-on-reset circuit (V_{POR}) that allows for an initial condition and the ramping of V_{CC} to set the internal logic.

As with the standard I^2C system, pullup resistors are required on each SDAn and SCLn to provide the logic high levels on the buffered bus. The size of these pullup resistors depends on the system, but it is essential that each side of the repeater have a pullup resistor. The device is designed to work with standard-mode and fast-mode I^2C devices in addition to SMBus devices. Standard-mode I^2C devices only specify 3 mA in a generic I^2C system where standard-mode devices and multiple masters are possible.

TERMINAL FUNCTIONS

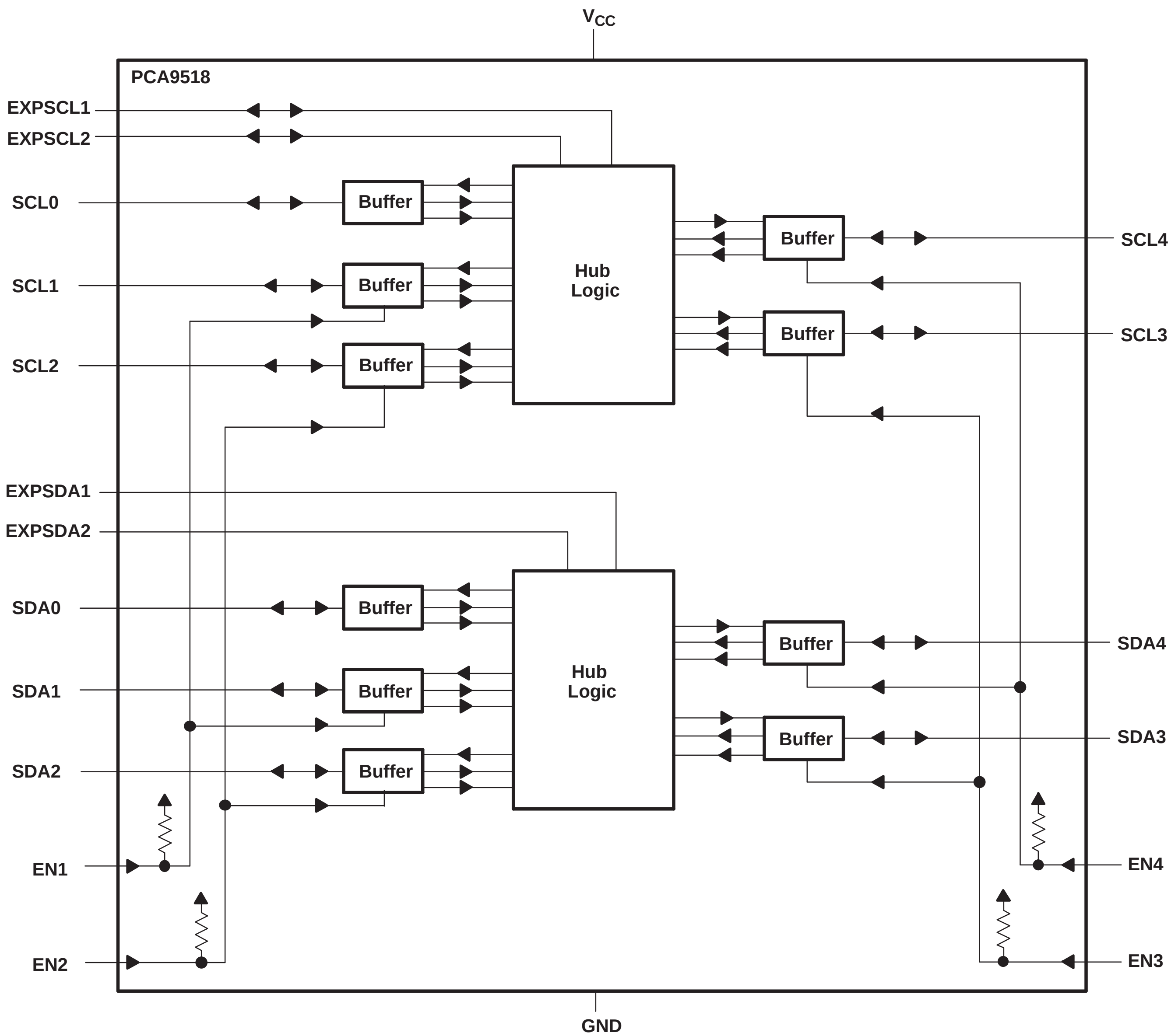
SOIC, SSOP, TSSOP, OR QSOP PIN NO.	NAME	DESCRIPTION
1	EXPSCL1	Expandable serial clock pin 1. Connect to V_{CC} through a pullup resistor.
2	EXPSCL2	Expandable serial clock pin 2. Connect to V_{CC} through a pullup resistor.
3	SCL0	Serial clock bus 0. Connect to V_{CC} through a pullup resistor.
4	SDA0	Serial data bus 0. Connect to V_{CC} through a pullup resistor.
5	SCL1	Serial clock bus 1. Connect to V_{CC} through a pullup resistor.
6	SDA1	Serial data bus 1. Connect to V_{CC} through a pullup resistor.
7	EN1	Active-high bus enable 1
8	SCL2	Serial clock bus 2. Connect to V_{CC} through a pullup resistor.
9	SDA2	Serial data bus 2. Connect to V_{CC} through a pullup resistor.
10	GND	Ground
11	EN2	Active-high bus enable 2
12	SCL3	Serial clock bus 3. Connect to V_{CC} through a pullup resistor.
13	SDA3	Serial data bus 3. Connect to V_{CC} through a pullup resistor.
14	EN3	Active-high bus enable 3
15	SCL4	Serial clock bus 4. Connect to V_{CC} through a pullup resistor.
16	SDA4	Serial data bus 4. Connect to V_{CC} through a pullup resistor.
17	EN4	Active-high bus enable 4
18	EXPSDA1	Expandable serial data pin 1. Connect to V_{CC} through a pullup resistor.
19	EXPSDA2	Expandable serial data pin 2. Connect to V_{CC} through a pullup resistor.
20	V_{CC}	Supply voltage

FUNCTION TABLE(1)(2)(3)

INPUTS				FUNCTION							
EN1	EN2	EN3	EN4	SCL1	SCL2	SCL3	SCL4	SDA1	SDA2	SDA3	SDA4
L	L	L	L	Disconnect	Disconnect	Disconnect	Disconnect	Disconnect	Disconnect	Disconnect	Disconnect
L	L	L	H	Disconnect	Disconnect	Disconnect	SCL0	Disconnect	Disconnect	Disconnect	SDA0
L	L	H	L	Disconnect	Disconnect	SCL0	Disconnect	Disconnect	Disconnect	SDA0	Disconnect
L	L	H	H	Disconnect	Disconnect	SCL0	SCL0	Disconnect	Disconnect	SDA0	SDA0
L	H	L	L	Disconnect	SCL0	Disconnect	Disconnect	Disconnect	SDA0	Disconnect	Disconnect
L	H	L	H	Disconnect	SCL0	Disconnect	SCL0	Disconnect	SDA0	Disconnect	SDA0
L	H	H	L	Disconnect	SCL0	SCL0	Disconnect	Disconnect	SDA0	SDA0	Disconnect
L	H	H	H	Disconnect	SCL0	SCL0	SCL0	Disconnect	SDA0	SDA0	SDA0
H	L	L	L	SCL0	Disconnect	Disconnect	Disconnect	SDA0	Disconnect	Disconnect	Disconnect
H	L	L	H	SCL0	Disconnect	Disconnect	SCL0	SDA0	Disconnect	Disconnect	SDA0
H	L	H	L	SCL0	Disconnect	SCL0	Disconnect	SDA0	Disconnect	SDA0	Disconnect
H	L	H	H	SCL0	Disconnect	SCL0	SCL0	SDA0	Disconnect	SDA0	SDA0
H	H	L	L	SCL0	SCL0	Disconnect	Disconnect	SDA0	SDA0	Disconnect	Disconnect
H	H	L	H	SCL0	SCL0	Disconnect	SCL0	SDA0	SDA0	Disconnect	SDA0
H	H	H	L	SCL0	SCL0	SCL0	Disconnect	SDA0	SDA0	SDA0	Disconnect
H	H	H	H	SCL0	SCL0	SCL0	SCL0	SDA0	SDA0	SDA0	SDA0

(1) SCL from master = SCL0
(2) SDA from master = SDA0
(3) See *Description* and *Application Information* for information on EXPxxx1 and EXPxxx2 behavior.

FUNCTIONAL BLOCK DIAGRAM



A more detailed view of each buffer in the functional block diagram is shown in Figure 1.

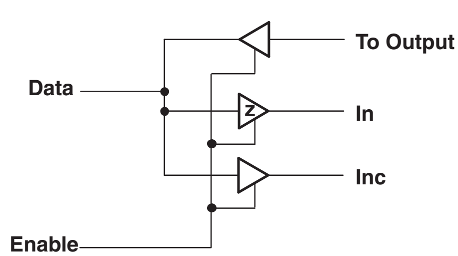


Figure 1. Buffer Details

Enable

EN1–EN4 are active-high enable pins and have internal pullup resistors. Each enable pin, ENn, controls its associated SDAn and SCLn ports. When ENn is low, it isolates its corresponding SDAn and SCLn from the system by blocking the inputs from SDAn and SCLn and disabling the output drivers on the SDAn and SCLn pins. It is essential that the ENn change state only when both the global bus and the local port are in an idle state to prevent system failures. EN1–EN4 also allow the use of open-drain drivers that can be wire-ORed to create a distributed enable where either centralized control signal (master) or spoke signal (submaster) can enable the channel when it is idle.

Expansion

The PCA9518 has four open-drain I/O pins used for expansion. The internal state of the serial data within each hub is communicated to other hubs through two expansion pins, EXPSDA1 and EXPSDA2. The EXPSDA1 pins of all hubs are connected together to form an open-drain bus. Similarly, all EXPSDA2 pins, EXPSCL1 pins, and EXPSCL2 pins are connected together, forming a 4-wire bus between hubs. When it is necessary to be able to deselect every port, each expansion device contributes only four ports that can be enabled or disabled; the fifth port does not have an enable pin. Pullup resistors are required on the EXPxxxx pins, even if only one PCA9518 is used.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{CC}	Supply voltage range			–0.5	7	V
V_I	Enable input voltage range[2]			–0.5	7	V
$V_{I/O}$	I^2C bus voltage range			–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$			–50	mA
I_{OK}	Output clamp current	$V_O < 0$			–50	mA
I_O	Continuous output current				±50	mA
	Continuous current through V_{CC} or GND				±100	mA
θ_{JA}	Package thermal impedance[3]	DB package			63	°C/W
		DBQ package			61	
		DW package			46	
		PW package			88	
T_{stg}	Storage temperature range			–55	125	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	SCL, SDA	$0.7 \times V_{CC}$		5.5	V
		EN	2		5.5	
		EXPSDA, EXPSCL	$0.55 \times V_{CC}$		5.5	
V_{IL}[1]	Low-level input voltage	SCL, SDA	–0.5		$0.3 \times V_{CC}$	V
		EN	–0.5		0.8	
		EXPSDA, EXPSCL	–0.5		$0.45 \times V_{CC}$	
V_{ILc}[1]	Low-level input voltage contention	SCL, SDA	–0.5		0.4	V
T_A	Operating free-air temperature		–40		85	°C

(1) V_{IL} specification is for the first low level seen by SDA/SCL. V_{ILc} is for the second and subsequent low levels seen by SDA/SCL. V_{ILc} must be at least 70 mV below V_{OL}.

Electrical Characteristics

over recommended operating free-air temperature range, V_{CC} = 3 V to 3.6 V, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA		3 V to 3.6 V			–1.2	V
V_{OL}	SCLn, SDAn	I_{OL} = 0(2) or 6 mA		3 V to 3.6 V	0.45	0.52	0.7	V
	EXPSCL, EXPSDA	I_{OL} = 12 mA		3 V to 3.6 V			0.5	
$V_{OL} – V_{ILc}$	Low-level input voltage below low-level output voltage	SCL, SDA		3 V to 3.6 V			70	mV
I_I	SCLn, SDAn	V_I = 3.6 V		3 V to 3.6 V			±1	μA
		V_I = 0.2 V					1	
	EN1, EN2, EN3, EN4	$V_I = V_{CC}$					±1	
		V_I = 0.2 V (input current LOW)				10	20	
	EXPSCL, EXPSDA	V_I = 0.2 V					2	
I_{CC}	Quiescent supply current, Both channels high	SDAn = SCLn = V_{CC}, EXPSCLn = EXPSDAn = V_{CC}		3.6 V		1.75	6	mA
	Quiescent supply current, Both channels low	One SDA and one SCL are at GND, while other SDA and SCL are open.				2.5	9	
	Quiescent supply current, In contention	SDAn = SCLn = GND, EXPSCLn = EXPSDAn = V_{CC}				9	11	
I_{off}	SDAx, SCLx power-off condition with static V_{CC}	V_I = 3.6 V	EN = L or H	0 V			1	μA
		VI = GND					1	
$I_{I(ramp)}$	SDAx, SCLx power-off condition with V_{CC} ramping up or down	V_I = 3.6 V,	EN = L or H	0 V to 3 V			1	μA
C_I	SCLn, SDAn	V_I = 3 V or GND		3 V to 3.6 V		8	9.5	pF
	EN1, EN2, EN3, EN4					3	7	
	EXPSCL, EXPSDA					6	8	

(1) All typical values are at 3.3-V supply voltage and T_A = 25°C.
(2) Test performed with I_{OL} = 10 μA

Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 2)[(1)]

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{PHLs} [(2)]	Propagation delay	SDA or SCL	SDAn or SCLn	105	202	389	ns
t_{PLHs} [(3)]				105	259	265	ns
t_{PHLE1s}		EXPSDA1 or EXPSCL1	SDA or SCL	109	193	327	ns
t_{PLHE1s}				120	153	200	ns
t_{PLHE2s}		EXPSDA2 or EXPSCL2	SDA or SCL	120	234	279	ns
t_{THLs}	Output transition time, SDAn, SCLn	70%	30%	48	110	187	ns
t_{TLHs}		30%	70%		0.85RC		ns

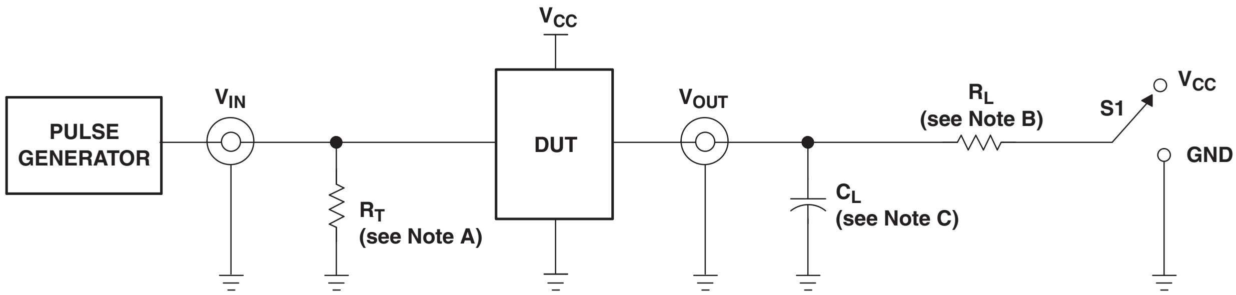
(1) The SDA and SCL propagation delays are dominated by rise times or fall times. The fall times mostly are internally controlled and are sensitive only to load capacitance. The rise times are RC time-constant controlled and, therefore, a specific numerical value can be given only for fixed RC time constants.
(2) The SDA high-to-low propagation delay, t_{PHLs}, includes the fall time from V_{CC} to 0.5 V_{CC} of EXPSDA1 or EXPSCL1 and the SDA or SCL fall time from the quiescent high (usually V_{CC}) to below 0.3 V_{CC}. The SDA and SCL outputs have edge-rate-control circuits included that make the fall time almost independent of load capacitance.
(3) The SDA or SCL low-to-high propagation delay, t_{PLHs}, includes the rise-time constant from the quiescent low to 0.5 V_{CC} for EXPSDA1 or EXPSCL2, the rise-time constant for the quiescent low to 0.5 V_{CC} for EXPSDA1 or EXPSCL1, and the rise time constant from the quiescent externally driven low to 0.7 V_{CC} for SDA or SCL.

Timing Requirements

over operating free-air temperature range (unless otherwise noted)

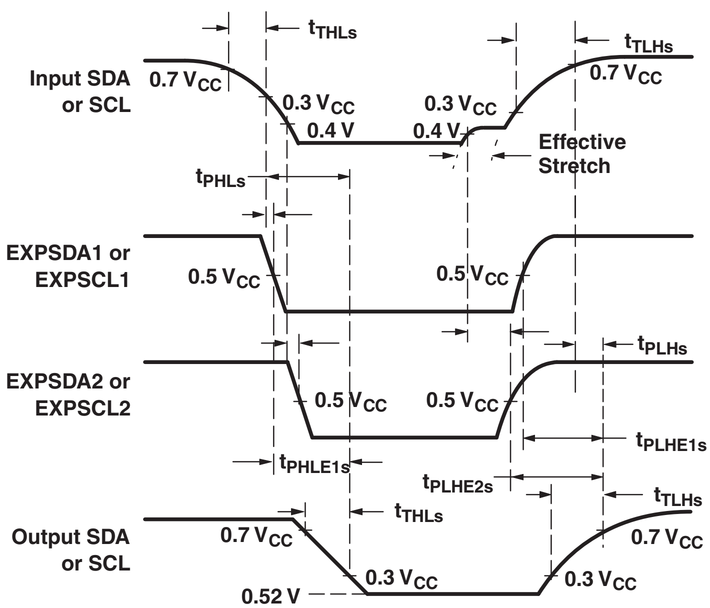
PARAMETER		MIN	MAX	UNIT
t_{su}	Setup time, EN↑ before Start condition	300		ns
t_h	Hold time, EN↓ after Stop condition	300		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT FOR OPEN-DRAIN OUTPUT

TEST	S1
t_{PLH}/t_{PHL}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

A. Termination resistance, R_T, should be equal to the Z_{OUT} of the pulse generators.

B. Load resistor, R_L = 1.1 kΩ for I²C and 500 Ω for EXP

C. Load capacitance, C_L, includes jig and probe capacitance; 100 pF for I²C and EXP.

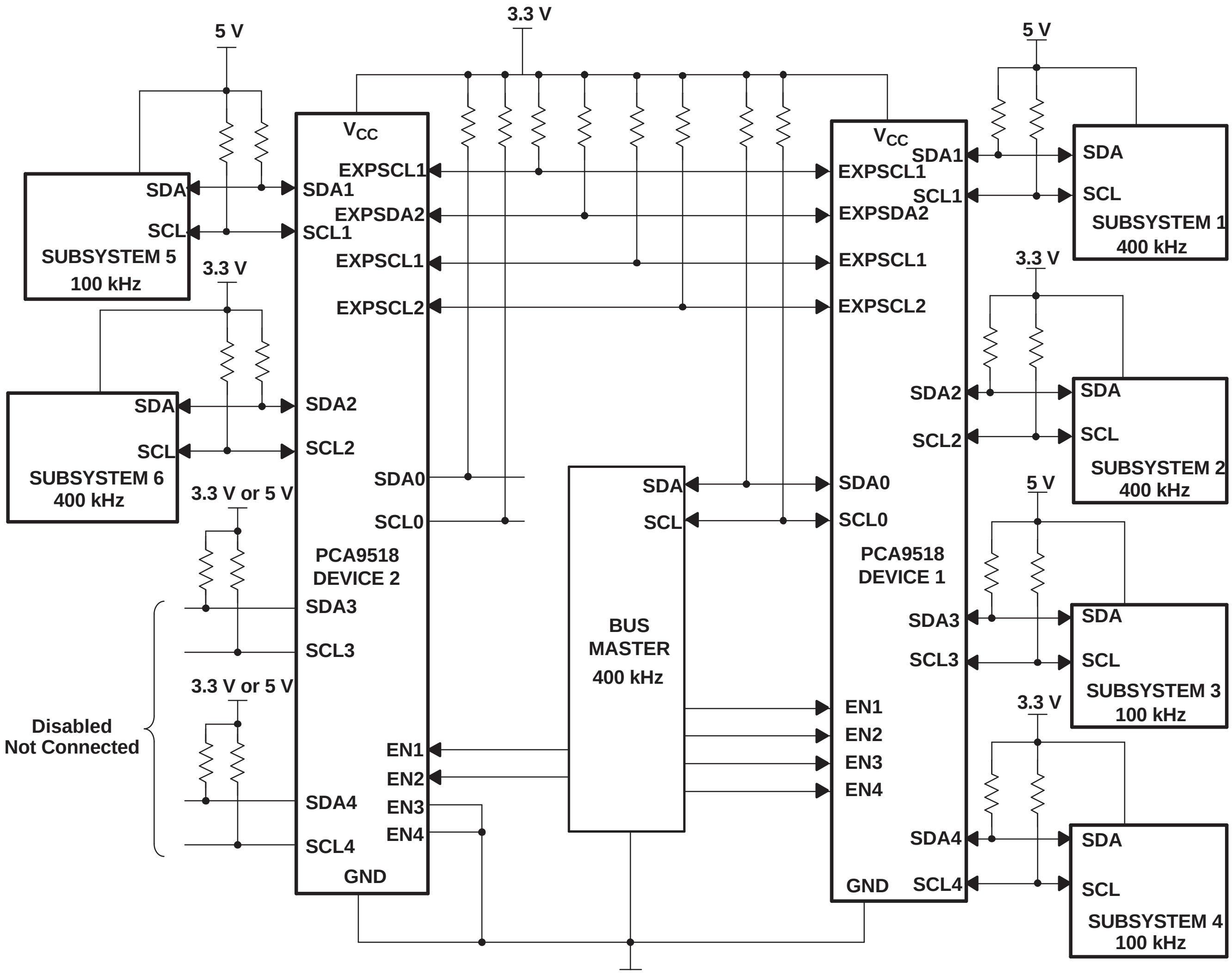
D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.

E. The outputs are measured one at a time, with one transition per measurement.

Figure 2. Test Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 3 shows an application in which the PCA9518 can be used.



A. Only two of the five channels of the PCA9518 device 2 are being used. EN3 and EN4 are connected to GND to disable channels 3 and 4, or SDA3/SCL3 and SDA4/SCL4 are pulled up to V_{CC}. SDA0 and SCL0 can be used as a normal I²C port, but they must be pulled up to V_{CC} if unused, because there is no enable pin.

Figure 3. Multiple Expandable Five-Channel I²C Hubs

Here, the system master is running on a 3.3-V I²C bus, while the slaves are connected to a 3.3-V or 5-V bus. The PCA9518 is 5-V tolerant, so it does not require any additional circuitry to translate between the different bus voltages.

All buses run at 100 kHz, unless slaves 3, 4, and 5 are isolated from the bus. If the master bus and slaves 1, 2, and 6 need to run at 400 kHz, slaves 3, 4, and 5 can be isolated through the bus master. In this case, the bus master will change the state on the corresponding EN pin (for slaves 3, 4, and 5) to low.

Any segment of the hub can talk to any other segment of the hub. Bus masters and slaves can be located on any segment with 400-pF load allowed on each segment.

When one port of the PCA9518 is pulled low by a device on the I²C bus, a CMOS hysteresis-type input detects the falling edge and drives the EXPxxx1 line low; when the EXPxxx1 voltage is less than 0.5-V V_{CC}, the other ports are pulled down to the V_{OL} of the PCA9518, which is typically 0.5 V.

APPLICATION INFORMATION (continued)

If the bus master in Figure 3 were to write to the slave through the PCA9518, the waveform shown in Figure 4 would be created.

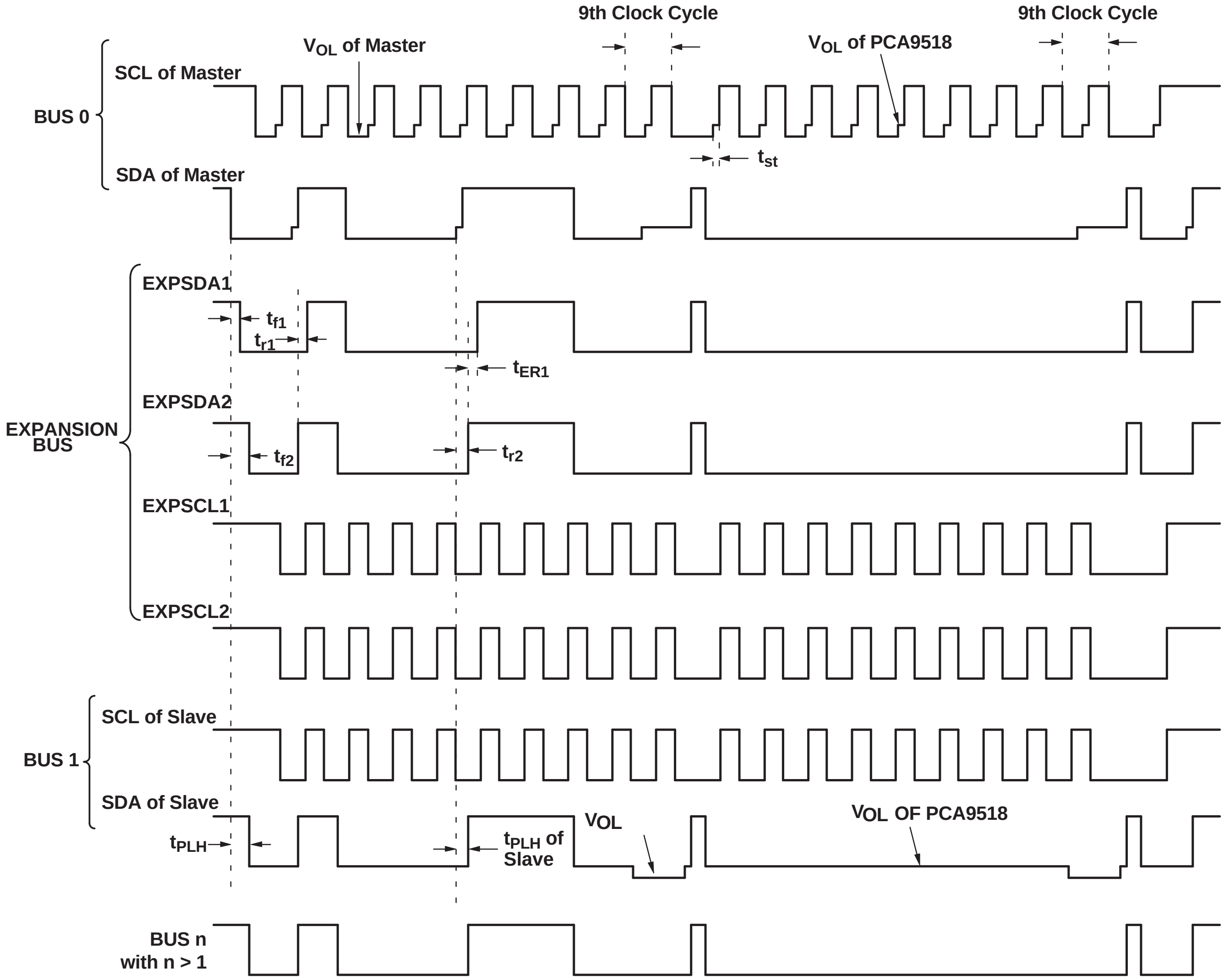


Figure 4. Bus Waveforms

Note that any arbitration or clock-stretching events on bus 1 require that the V_{OL} of the devices on bus 1 be 70 mV below the V_{OL} of the PCA9518 (see V_{OL} – V_{ILc} in electrical characteristics) to be recognized by the PCA9518 and transmitted to bus 0.

This looks like a normal I²C transmission, except for the small step preceding each clock low-to-high transition and proceeding each data low-to-high transition for the master. The step height is the difference between the low level driven by the master and the higher-voltage low level driven by the PCA9518 repeater. Its width corresponds to an effective clock stretching coming from the PCA9518, which delays the rising edge of the clock. That same magnitude of delay is seen on the rising edge of the data. The step on the rising edge of the data is extended through the ninth clock pulse as the PCA9518 repeats the acknowledge from the slave to the master. The clock of the slave looks normal, except that the V_{OL} is the 0.5-V level generated by the PCA9518. The SDA at the slave has a particularly interesting shape during the ninth clock cycle, when the slave pulls the line below the value driven by the PCA9518 during the ACK and then returns to the PCA9518 level, creating a foot before it completes the low-to-high transition. SDA lines, other than the one with the master and the one with the slave, have a uniform low level driven by the PCA9518 repeater.

APPLICATION INFORMATION (continued)

The expansion bus signals shown in Figure 4 are included primarily for timing reference points.

All timing on the expansion bus is with respect to 0.5 V_{CC}. EXPSDA1 is driven low whenever any SDA pin falls below 0.3-V V_{CC} and EXPSDA2 is driven low when any pin is ≤0.4 V. EXPSCL1 is driven LOW whenever any SCL pin falls below 0.3-V V_{CC} and EXPSCL2 is driven LOW when any SCL pin is ≤0.4 V. EXPSDA2 returns high after the SDA pin that was the last one being held below 0.4 V by an external driver starts to rise. The last SDA to rise above 0.4 V is held down by the PCA9518 to 0.5 V until after the delay of the circuit that determines that it was the last to rise; then, it is allowed to rise above the 0.5-V level driven by the PCA9518.

Considering the bus 0 SDA to be the last one to go above 0.4 V, then EXPSDA1 returns to high after EXPSDA2 is high and either bus 0 SDA rise time is 1 μs or bus 0 SDA reaches 0.7-V V_{CC}, whichever occurs first. After both EXPSDA2 and EXPSDA1 are high, the rest of the SDA lines are allowed to rise. The same description applies to the EXPSCL1, EXPSCL2, and SCL pins.

Any arbitration or clock stretching events on bus 1 requires that the V_{OL} of the devices on bus 1 be 70 mV below the V_{OL} of the PCA9518 (see V_{OL} – V_{ILc} in electrical characteristics) to be recognized by the PCA9518 and then transmitted to bus 0.

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
PCA9518DBQR	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9518DBQRG4	ACTIVE	SSOP/ QSOP	DBQ	20	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
PCA9518DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518DBT	ACTIVE	SSOP	DB	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518DBTG4	ACTIVE	SSOP	DB	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518DWT	ACTIVE	SOIC	DW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518DWTG4	ACTIVE	SOIC	DW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
PCA9518PWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

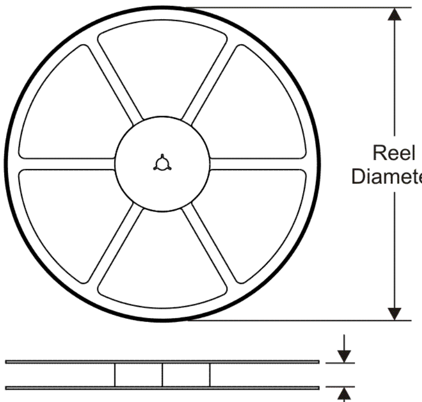
[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

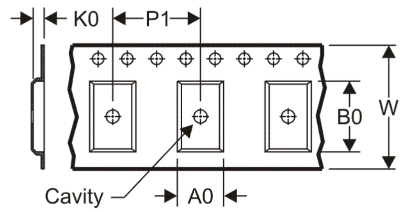
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

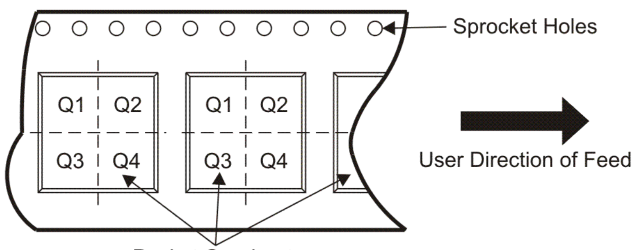


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

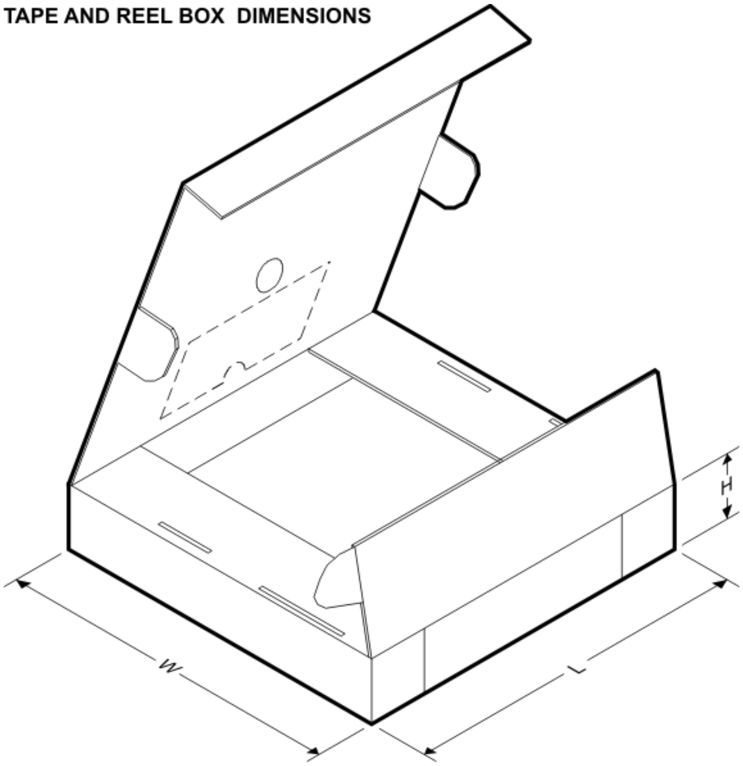
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9518DBQR	SSOP/ QSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCA9518DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
PCA9518DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
PCA9518PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCA9518PWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

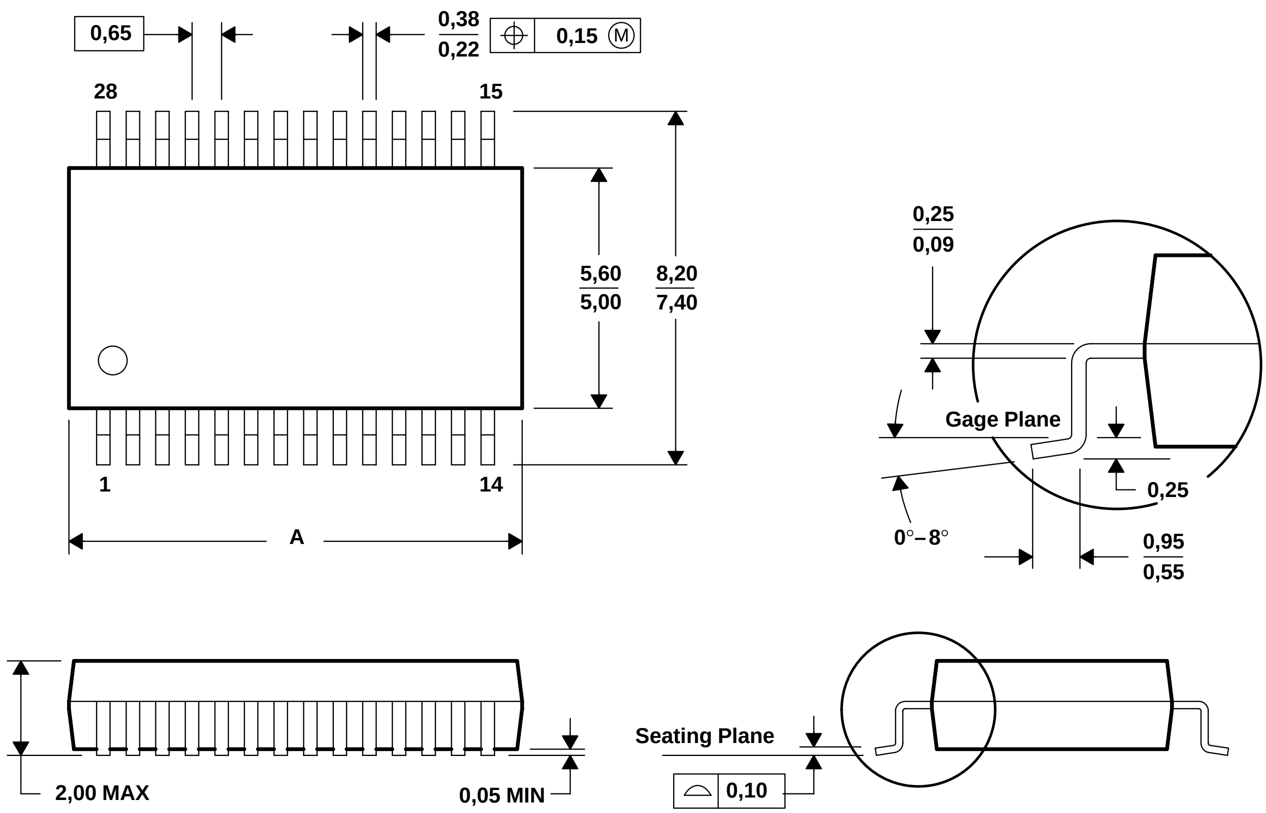


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9518DBQR	SSOP/QSOP	DBQ	20	2500	346.0	346.0	33.0
PCA9518DBR	SSOP	DB	20	2000	346.0	346.0	33.0
PCA9518DWR	SOIC	DW	20	2000	346.0	346.0	41.0
PCA9518PWR	TSSOP	PW	20	2000	346.0	346.0	33.0
PCA9518PWT	TSSOP	PW	20	250	346.0	346.0	33.0

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



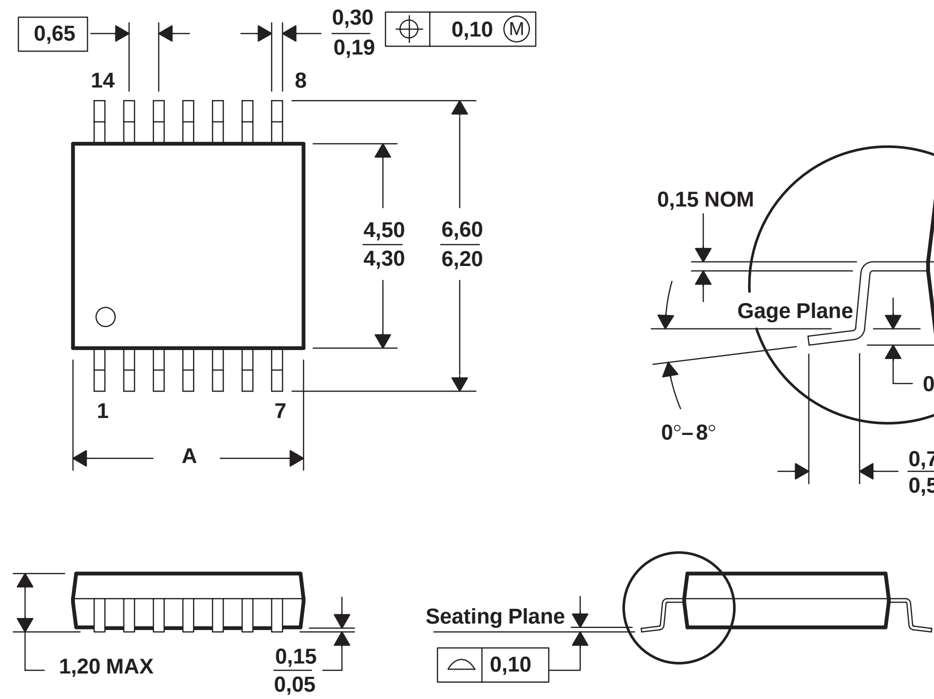
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

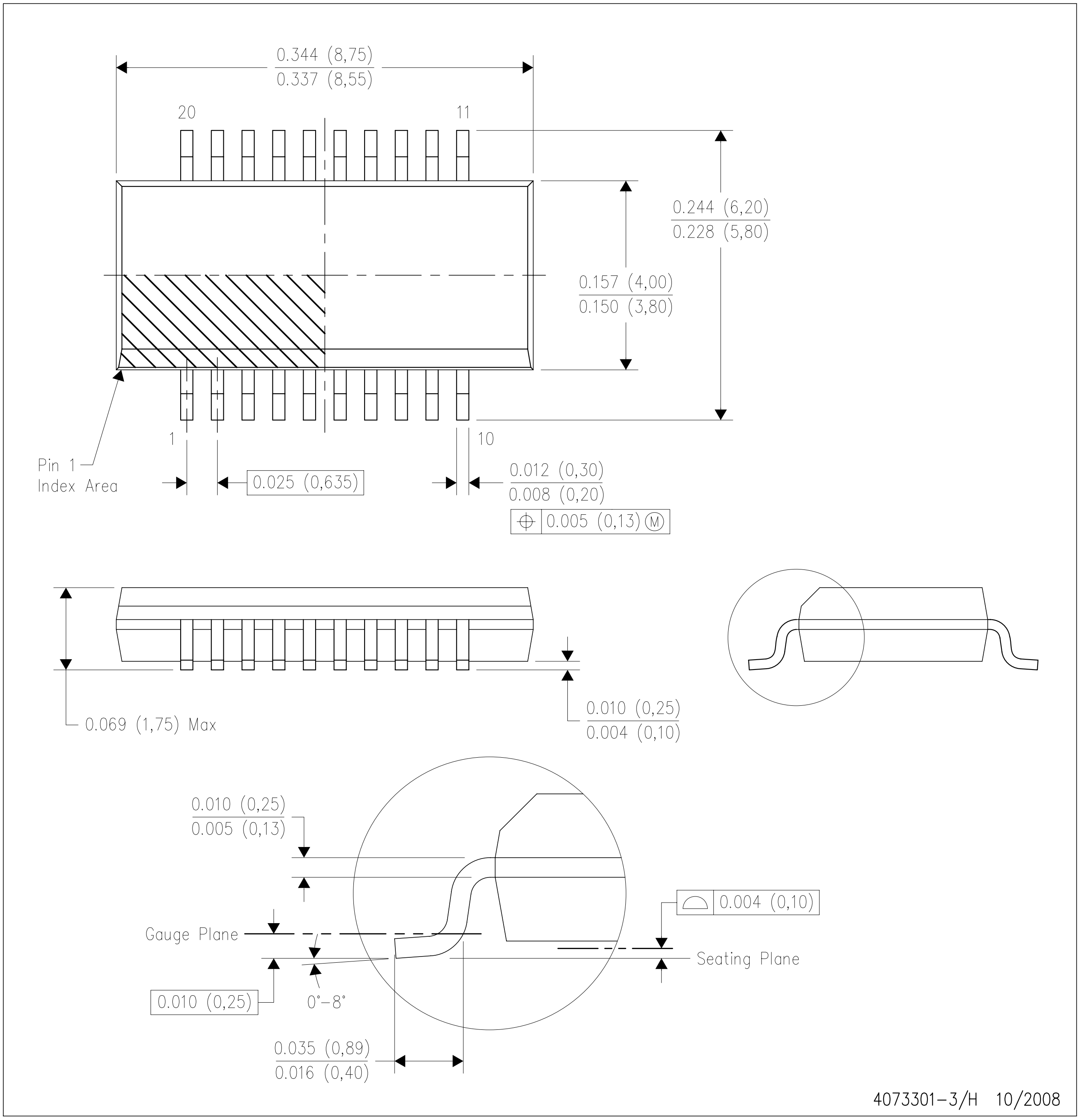


PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

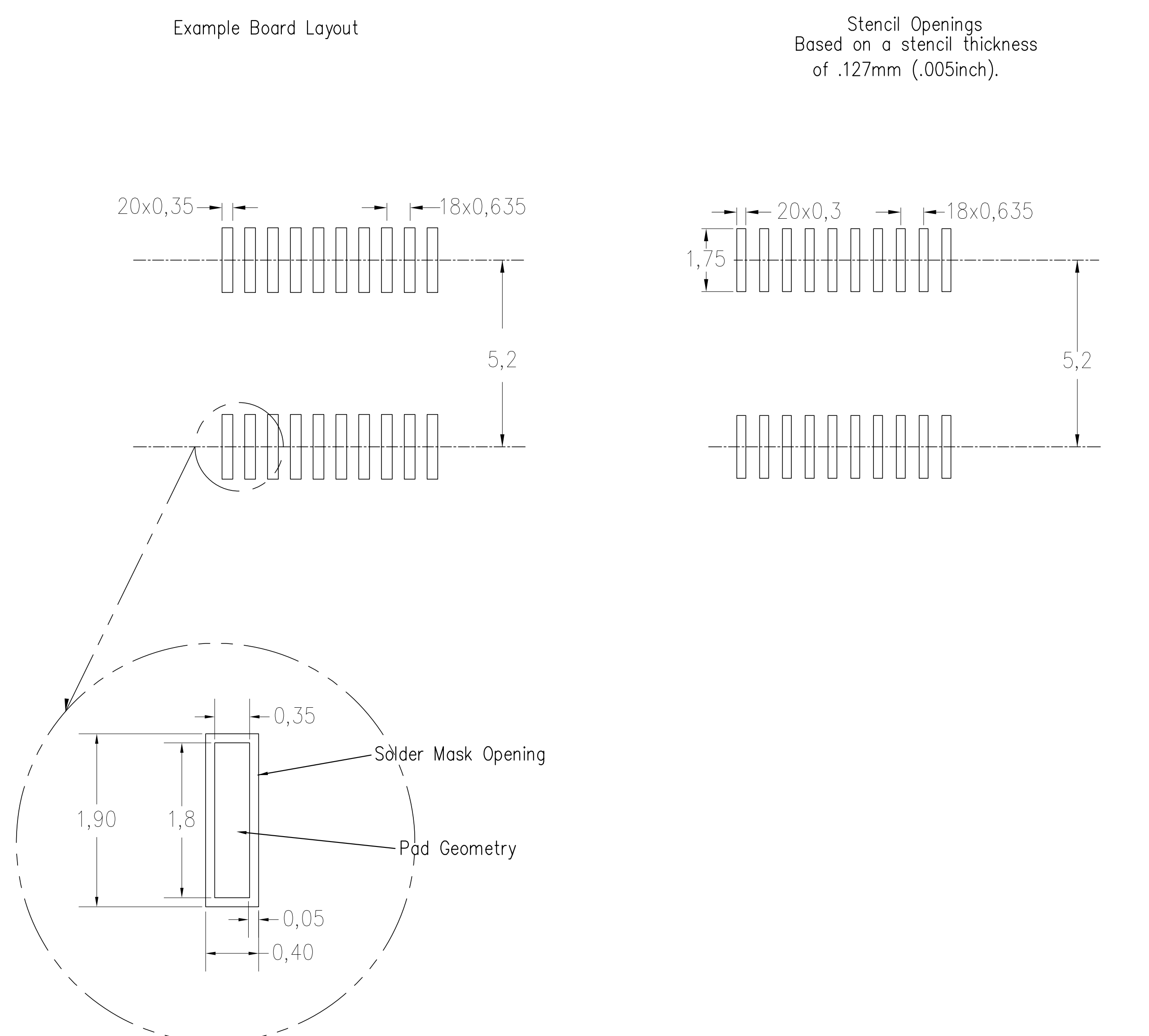
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

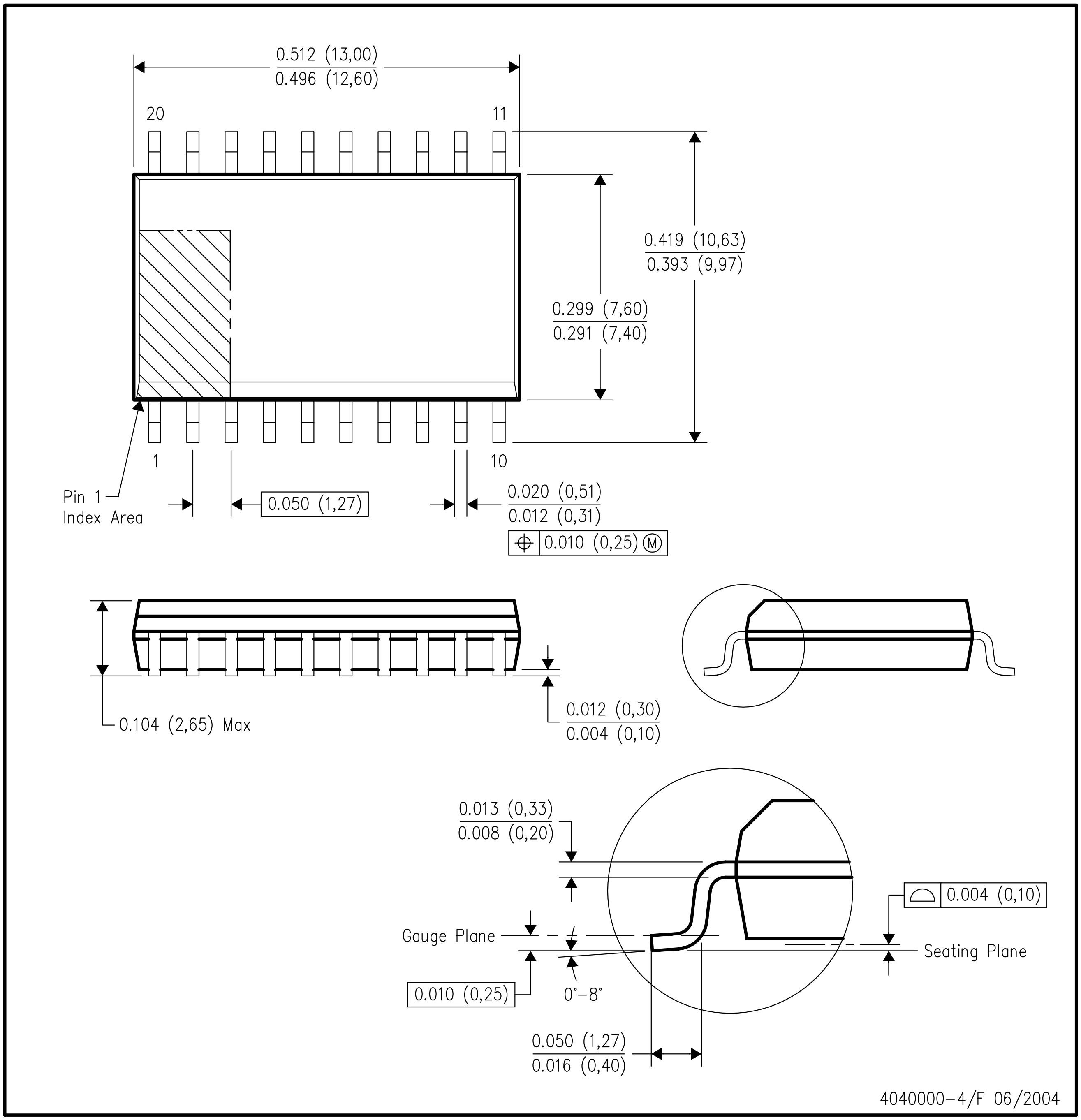
DBQ (R-PDSO-G20)



4210335-3/A 06/09

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DW (R-PDSO-G20) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.