



0.05 μ V/ $^{\circ}$ C max, SINGLE-SUPPLY CMOS OPERATIONAL AMPLIFIERS Zero-Drift Series

FEATURES

- LOW OFFSET VOLTAGE: 5 μ V (max)
- ZERO DRIFT: 0.05 μ V/ $^{\circ}$ C max
- QUIESCENT CURRENT: 750 μ A (max)
- SINGLE-SUPPLY OPERATION
- LOW BIAS CURRENT: 200pA (max)
- SHUTDOWN
- *Micro*SIZE PACKAGES
- WIDE SUPPLY RANGE: 2.7V to 12V

APPLICATIONS

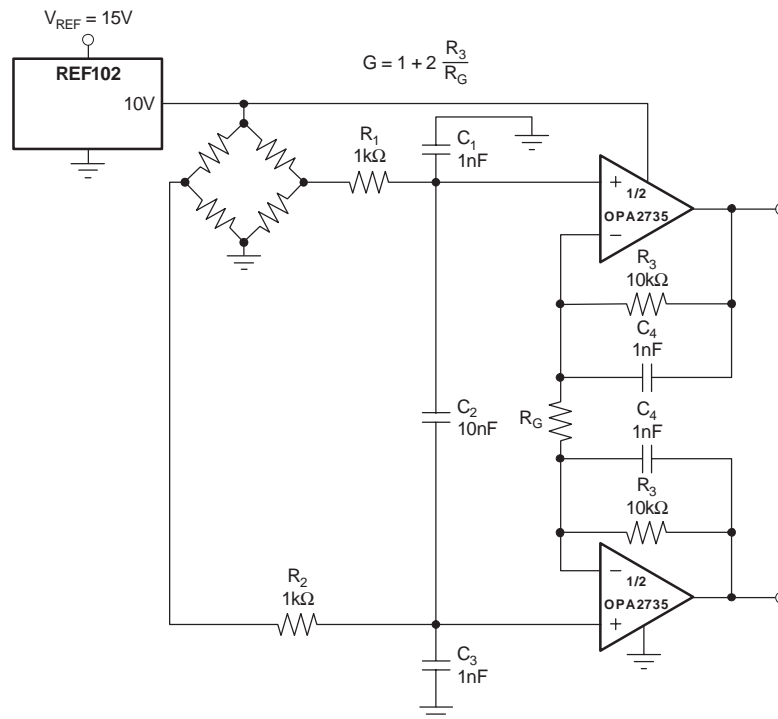
- TRANSDUCER APPLICATIONS
- TEMPERATURE MEASUREMENTS
- ELECTRONIC SCALES
- MEDICAL INSTRUMENTATION
- BATTERY-POWERED INSTRUMENTS
- HANDHELD TEST EQUIPMENT

DESCRIPTION

The OPA734 and OPA735 series of CMOS operational amplifiers use auto-zeroing techniques to simultaneously provide low offset voltage (5 μ V max) and near-zero drift over time and temperature. These miniature, high-precision, low quiescent current amplifiers offer high input impedance and rail-to-rail output swing within 50mV of the rails. Either single or bipolar supplies can be used in the range of +2.7V to +12V (\pm 1.35V to \pm 6V). They are optimized for low-voltage, single-supply operation.

The OPA734 family includes a shutdown mode. Under logic control, the amplifiers can be switched from normal operation to a standby current that is 9 μ A (max) and the output placed in a high-impedance state.

The single version is available in the *Micro*SIZE SOT23-5 (SOT23-6 for shutdown version) and the SO-8 packages. The dual version is available in the MSOP-8 and SO-8 packages (MSOP-10 only for the shutdown version). All versions are specified for operation from -40° C to $+85^{\circ}$ C.



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ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|----------------------------|
| Supply Voltage | +13.2V |
| Signal Input Terminals, Voltage ⁽²⁾ | (V-) – 0.5V to (V+) + 0.5V |
| Current ⁽²⁾ | ±10mA |
| Output Short Circuit ⁽³⁾ | Continuous |
| Operating Temperature | –40°C to +150°C |
| Storage Temperature | –65°C to +150°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| ESD Rating (Human Body Model), OPA734 | 1000V |
| ESD Rating (Human Body Model), OPA735, OPA2734, OPA2735 | 2000V |



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR(1) | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|-----------------------------|--------------|-----------------------|-----------------------------|-----------------|-----------------|---------------------------|
| Shutdown Version | | | | | | |
| OPA734 | SOT23-6 | DBV | –40°C to +85°C | NSB | OPA734AIDBVT | Tape and Reel, 250 |
| " | " | " | " | " | OPA734AIDBVR | Tape and Reel, 3000 |
| OPA734 | SO-8 | D | –40°C to +85°C | OPA734A | OPA734AID | Rails, 100 |
| " | " | " | " | " | OPA734AIDR | Tape and Reel, 2500 |
| OPA2734 | MSOP-10 | DGS | –40°C to +85°C | BGO | OPA2734AIDGST | Tape and Reel, 250 |
| " | " | " | " | " | OPA2734AIDGSR | Tape and Reel, 2500 |
| Non-Shutdown Version | | | | | | |
| OPA735 | SOT23-5 | DBV | –40°C to +85°C | NSC | OPA735AIDBVT | Tape and Reel, 250 |
| " | " | " | " | " | OPA735AIDBVR | Tape and Reel, 3000 |
| OPA735 | SO-8 | D | –40°C to +85°C | OPA735A | OPA735AID | Rails, 100 |
| " | " | " | " | " | OPA735AIDR | Tape and Reel, 2500 |
| OPA2735 | SO-8 | D | –40°C to +85°C | OPA2735A | OPA2735AID | Rails, 100 |
| " | " | " | " | " | OPA2735AIDR | Tape and Reel, 2500 |
| OPA2735 | MSOP-8 | DGK | –40°C to +85°C | BGN | OPA2735AIDGKT | Tape and Reel, 250 |
| " | " | " | " | " | OPA2735AIDGKR | Tape and Reel, 2500 |

(1) For the most current specification and package information, refer to our web site at www.ti.com.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ ($V_S = +10V$)

Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

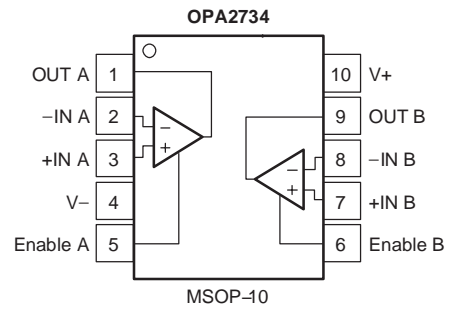
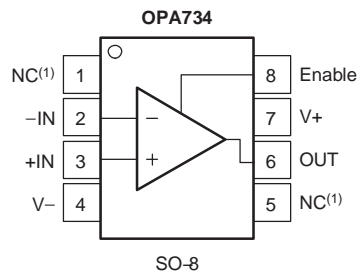
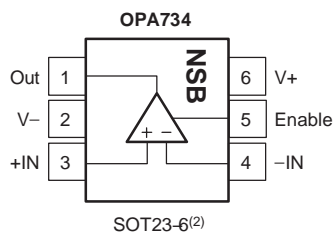
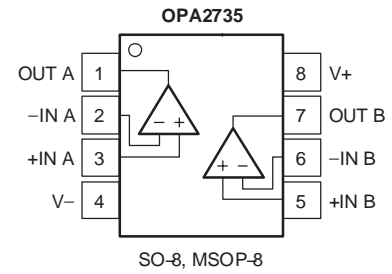
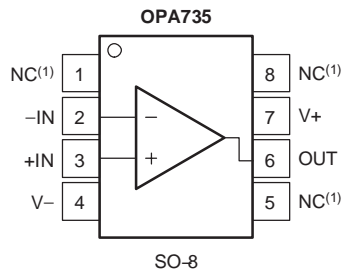
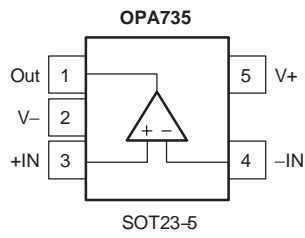
At $T_A = +25^\circ\text{C}$, $R_L = 10\text{k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

| PARAMETER | CONDITIONS | OPA734, OPA2734, OPA735, OPA2735 | | | UNIT |
|--|---|----------------------------------|---|-----------------------------|---|
| | | MIN | TYP | MAX | |
| OFFSET VOLTAGE Input Offset Voltage vs Temperature vs Power Supply Long-Term Stability Channel Separation, dc | V_{OS} dV_{OS}/dT PSRR $V_S = 2.7V$ to $12V$, $V_{CM} = 0V$ | | 1 0.01 0.2 Note (1) 0.1 | 5 0.05 1.8 | μV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/\text{V}$ $\mu\text{V}/\text{V}$ |
| INPUT BIAS CURRENT Input Bias Current over Temperature Input Offset Current | I_B $V_{CM} = V_S/2$ I_{OS} $V_{CM} = V_S/2$ | | See Typical Characteristics | | pA pA pA |
| NOISE Input Voltage Noise, $f = 0.01\text{Hz}$ to 1Hz Input Voltage Noise, $f = 0.1\text{Hz}$ to 10Hz Input Voltage Noise Density, $f = 1\text{kHz}$ Input Current Noise Density, $f = 1\text{kHz}$ | e_n e_n e_n i_n | | 1 3 150 40 | | μV_{PP} μV_{PP} $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$ |
| INPUT VOLTAGE RANGE Common-Mode Voltage Range Common-Mode Rejection Ratio | V_{CM} CMRR $(V^-) - 0.1V < V_{CM} < (V^+) - 1.5V$ | $(V^-) - 0.1$ 115 | 130 | $(V^+) - 1.5$ | V dB |
| INPUT CAPACITANCE Differential Common-Mode | | | 2 10 | | pF pF |
| OPEN-LOOP GAIN Open-Loop Voltage Gain | A_{OL} $(V^-) + 100\text{mV} < V_O < (V^+) - 100\text{mV}$ | 115 | 130 | | dB |
| FREQUENCY RESPONSE Gain-Bandwidth Product Slew Rate | GBW SR $G = +1$ | | 1.6 1.5 | | MHz V/ μs |
| OUTPUT Voltage Output Swing from Rail Short-Circuit Current Open-Loop Output Impedance Capacitive Load Drive | I_{SC} $R_L = 10\text{k}\Omega$ $f = 1\text{MHz}$, $I_O = 0$ C_{LOAD} | | 20 ± 20 125 | 50 | mV mA Ω |
| ENABLE/SHUTDOWN t_{OFF} $t_{ON}^{(2)}$ V_L (amplifier is shutdown) V_H (amplifier is active) I_{QSD} (per amplifier) Input Bias Current of Enable Pin | | V^- $(V^-) + 2$ | 1.5 150 4 3 | $(V^-) + 0.8$ V^+ 9 | μs μs V V μA μA |
| POWER SUPPLY Operating Voltage Range Quiescent Current (per amplifier) | V_S I_Q $I_Q = 0$ | | 2.7 to 12 (± 1.35 to ± 6) 0.6 | | V mA |
| TEMPERATURE RANGE Specified Range Operating Range Storage Range Thermal Resistance SOT23-5, SOT23-6 MSOP-8, MSOP-10, SO-8 | θ_{JA} | -40 -40 -65 | | +85 +150 +150 | $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$ |

(1) 300-hour life test at 150°C demonstrated randomly distributed variation in the range of measurement limits—approximately $1\mu\text{V}$.

(2) Device requires one complete auto-zero cycle to return to V_{OS} accuracy.

PIN CONFIGURATIONS



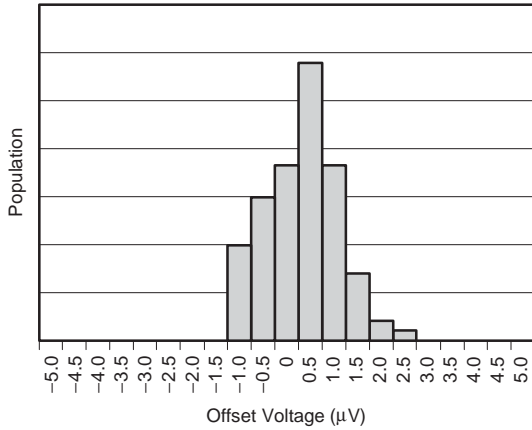
(1) NC = No Connection

(2) Pin 1 of the SOT23-6 is determined by orienting the package marking as shown in the diagram.

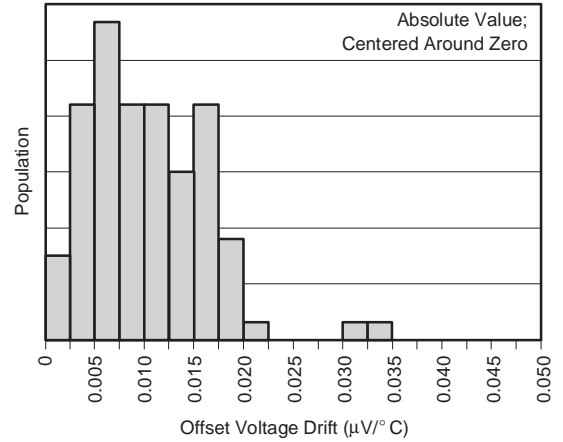
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ (same as $+10\text{V}$).

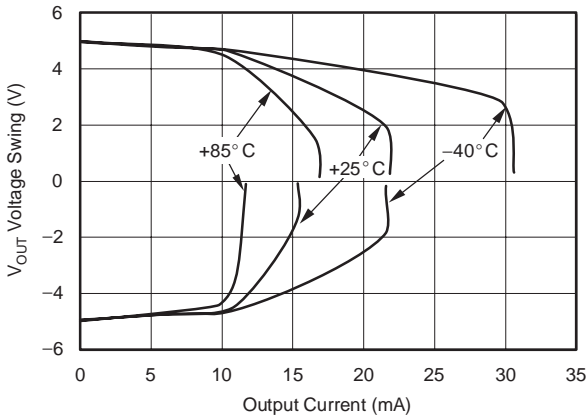
OUTPUT VOLTAGE PRODUCTION DISTRIBUTION



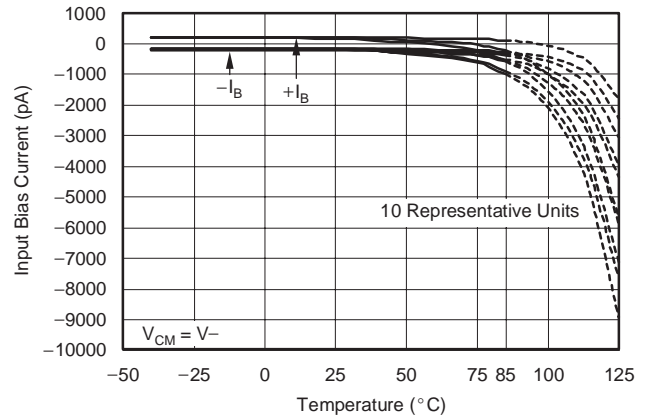
OUTPUT VOLTAGE DRIFT PRODUCTION DISTRIBUTION



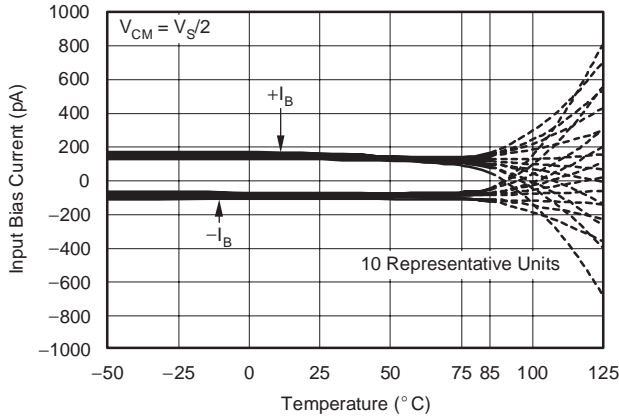
OUTPUT VOLTAGE SWING TO RAIL
vs OUTPUT CURRENT



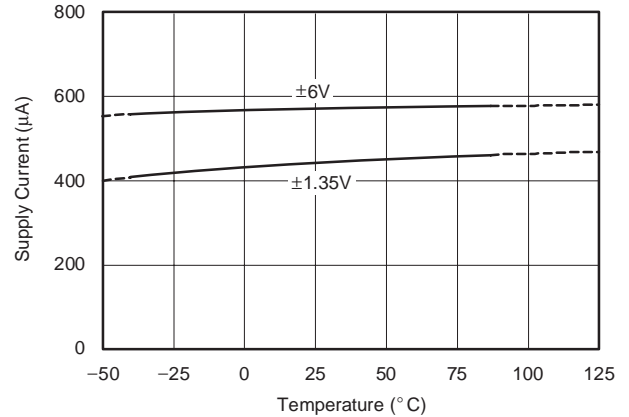
INPUT BIAS CURRENT vs TEMPERATURE



INPUT BIAS CURRENT vs TEMPERATURE

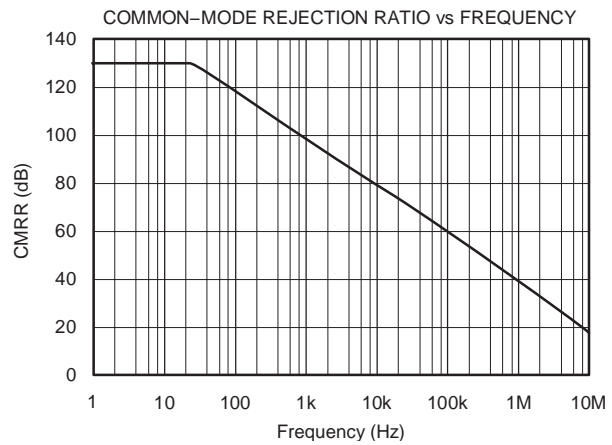
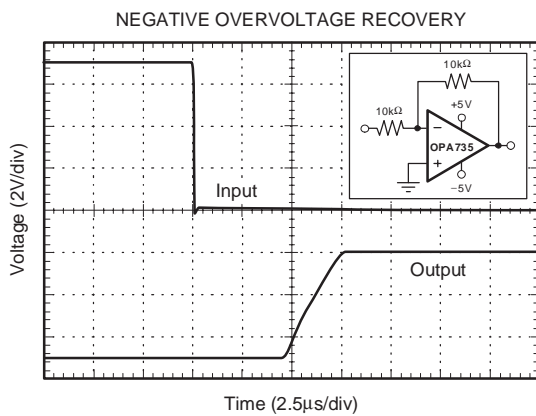
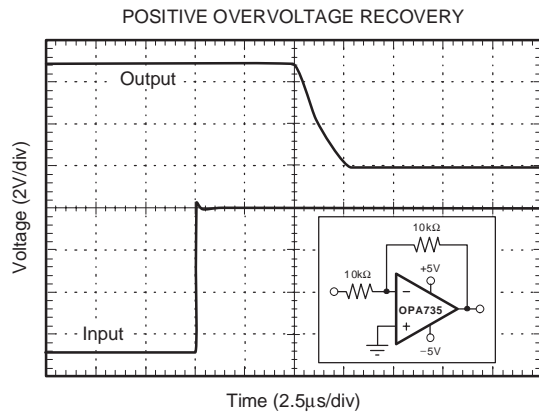
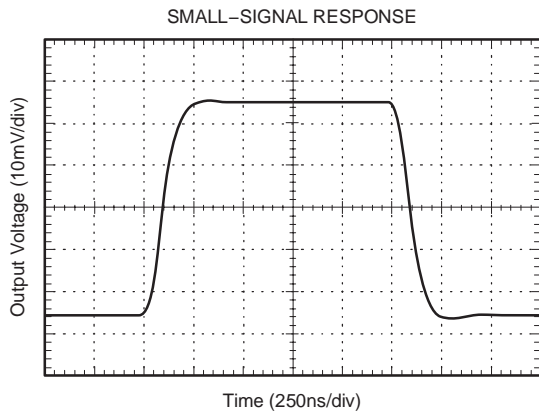
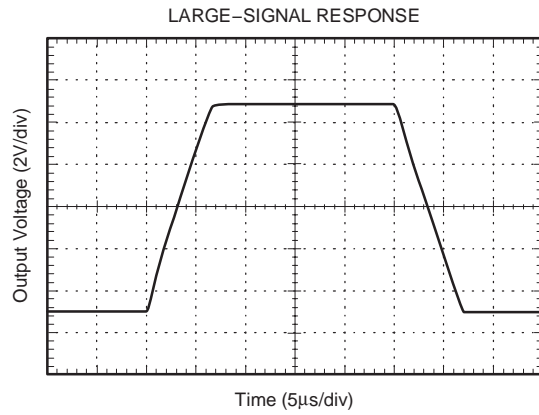
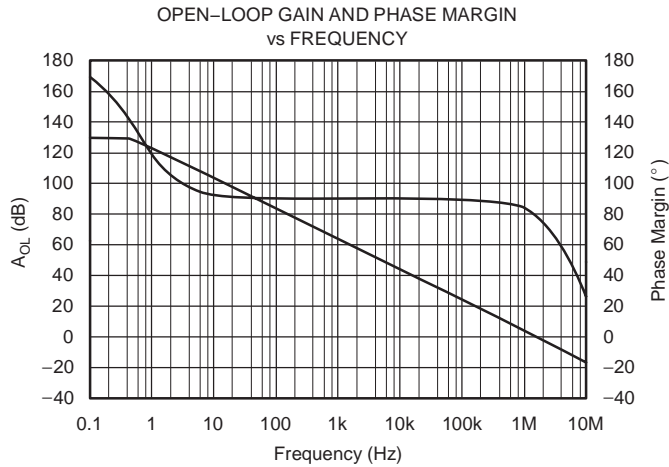


SUPPLY CURRENT vs TEMPERATURE



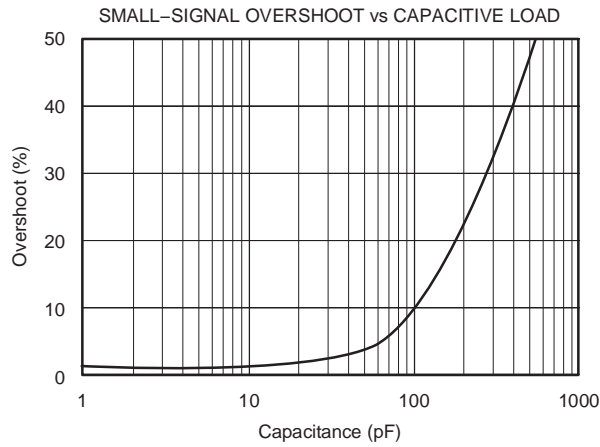
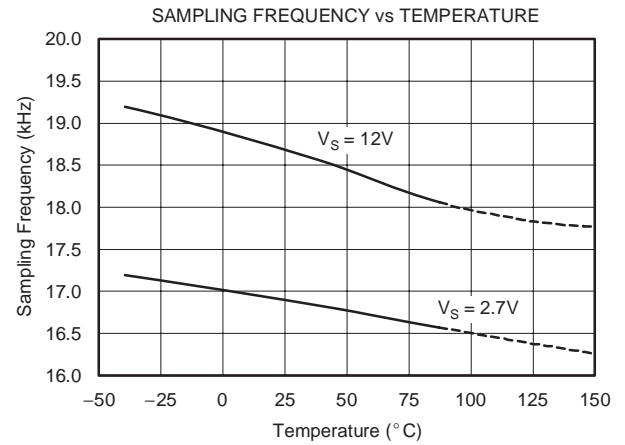
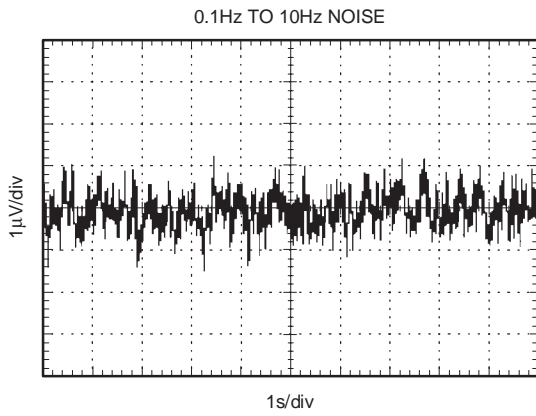
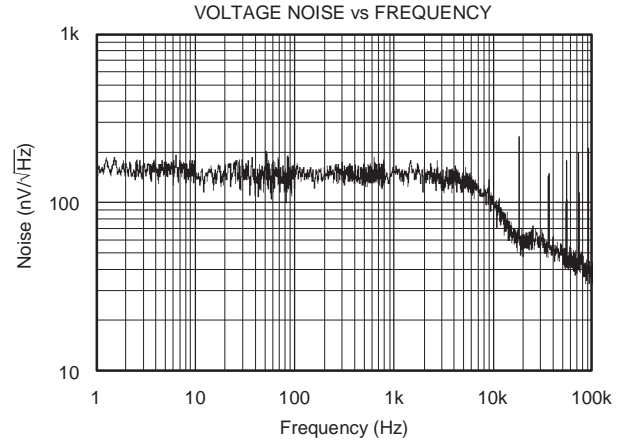
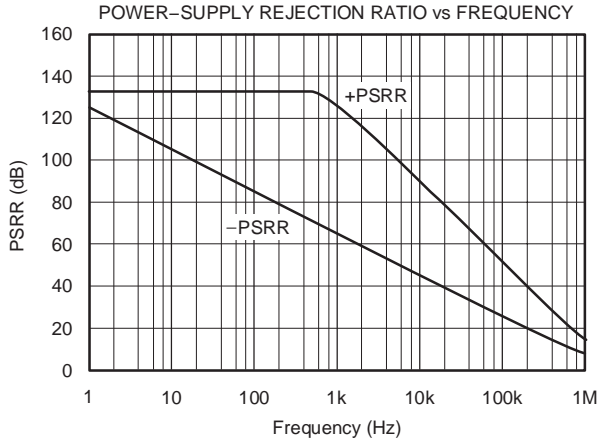
TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ (same as +10V).



TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 5\text{V}$ (same as +10V).



APPLICATIONS INFORMATION

The OPA734 and OPA735 series of op amps are unity-gain stable and free from unexpected output phase reversal. They use auto-zeroing techniques to provide low offset voltage and demonstrate very low drift over time and temperature.

Good layout practice mandates the use of a 0.1µF capacitor placed closely across the supply pins.

For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by assuring that they are equal on both input terminals:

1. Use low thermoelectric-coefficient connections (avoid dissimilar metals).
2. Thermally isolate components from power supplies or other heat sources.
3. Shield op amp and input circuitry from air currents such as cooling fans.

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1µV/°C or higher, depending on the materials used.

OPERATING VOLTAGE

The OPA734 and OPA735 op amp family operates with a power-supply range of +2.7V to +12V (±1.35V to ±6V). Supply voltages higher than +13.2V (absolute maximum) can permanently damage the amplifier. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

OPA734 ENABLE FUNCTION

The enable/shutdown digital input is referenced to the V₋ supply voltage of the op amp. A logic HIGH enables the op amp. A valid logic HIGH is defined as > (V₋) + 2V. The valid logic HIGH signal can be up to the positive supply, independent of the negative power supply voltage. A valid logic LOW is defined as < 0.8V above the V₋ supply pin. If dual or split power supplies are used, be sure that logic input signals are properly referred to the negative supply voltage. The Enable pin is connected to internal pull-up circuitry and will enable the device if this pin is left open circuit.

The logic input is a CMOS input. Separate logic inputs are provided for each op amp on the dual version. For battery-operated applications, this feature can be used to greatly reduce the average current and extend battery life.

The enable time is 150µs, which includes one full auto-zero cycle required by the amplifier to return to V_{OS} accuracy. Prior to returning to full accuracy, the amplifier may function properly, but with unspecified offset voltage.

Disable time is 1.5µs. When disabled, the output assumes a high-impedance state. The disable state allows the OPA734 to be operated as a gated amplifier, or to have the output multiplexed onto a common analog output bus.

INPUT VOLTAGE

The input common-mode range extends from (V₋) – 0.1V to (V₊) – 1.5V. For normal operation, the inputs must be limited to this range. The common-mode rejection ratio is only valid within the specified input common-mode range. A lower supply voltage results in lower input common-mode range; therefore, attention to these values must be given when selecting the input bias voltage. For example, when operating on a single 3V power supply, common-mode range is from 0.1V below ground to half the power-supply voltage.

Normally, input bias current is approximately 100pA; however, input voltages exceeding the power supplies can cause excessive current to flow in or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10mA. This is easily accomplished with an input resistor, as shown in Figure 1.

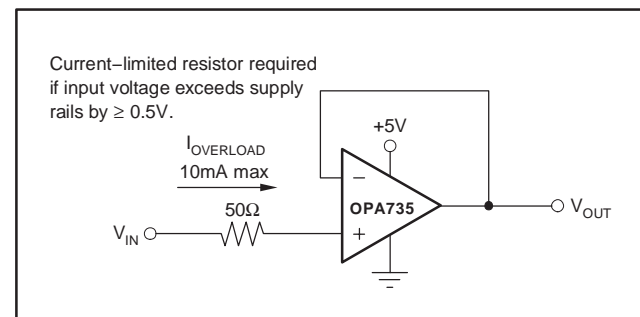


Figure 1. Input Current Protection

INTERNAL OFFSET CORRECTION

The OPA734 and OPA735 series of op amps use an auto-zero topology with a time-continuous 1.6MHz op amp in the signal path. This amplifier is zero-corrected every 100µs using a proprietary technique. Upon power-up, the amplifier requires one full auto-zero cycle of approximately 100µs in addition to the start-up time for the bias circuitry to achieve specified V_{OS} accuracy. Prior to this time, the amplifier may function properly but with unspecified offset voltage.

Low-gain (< 20) operation demands that the auto-zero circuitry correct for common-mode rejection errors of the main amplifier. Because these errors can be larger than 0.1% of a full-scale input step change, one calibration cycle (100μs) can be required to achieve full accuracy.

The term *clock feedthrough* describes the presence of the clock frequency in the output spectrum. In auto-zeroed op amps, clock feedthrough may result from the settling of the internal sampling capacitor, or from the small amount of charge injection that occurs during the sample-and-hold of the op amp offset voltage. Feedthrough can be minimized by keeping the source impedance relatively low (< 1kΩ) and matching the source impedance on both input terminals. If the source resistance is high (> 1kΩ) feedthrough can generally be reduced with a capacitor of 1nF or greater in parallel with the source or feedback resistors. See the circuit application examples.

LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short. When possible, use a PCB ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

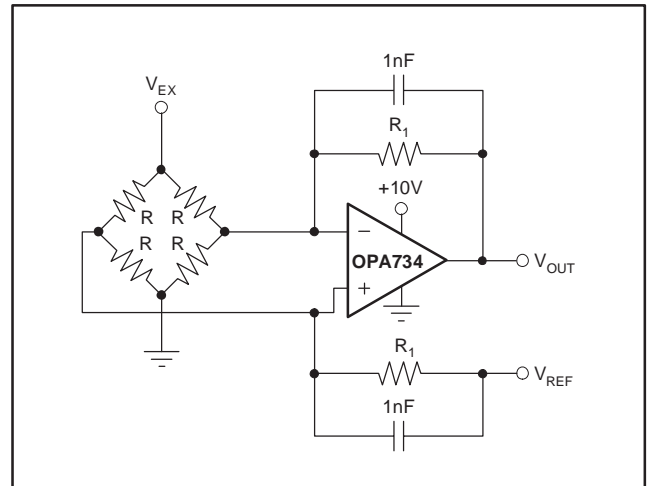
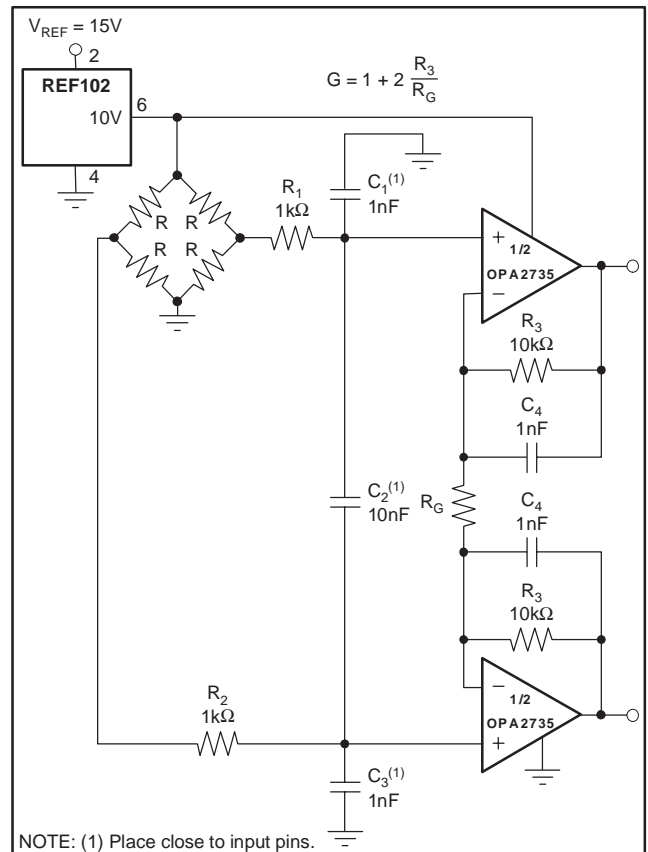


Figure 2. Single Op Amp Bridge Amplifier Circuit



NOTE: (1) Place close to input pins.

Figure 3. Differential Output Bridge Amplifier

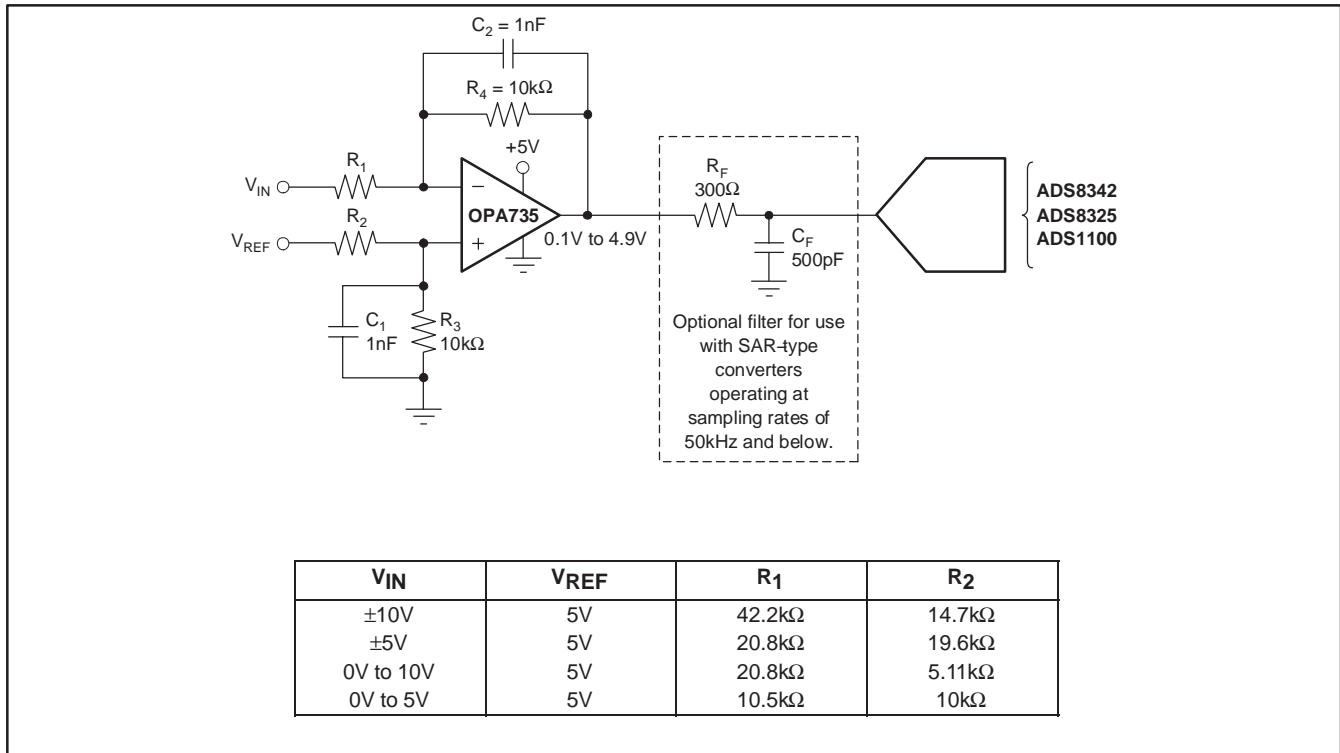


Figure 4. Driving ADC

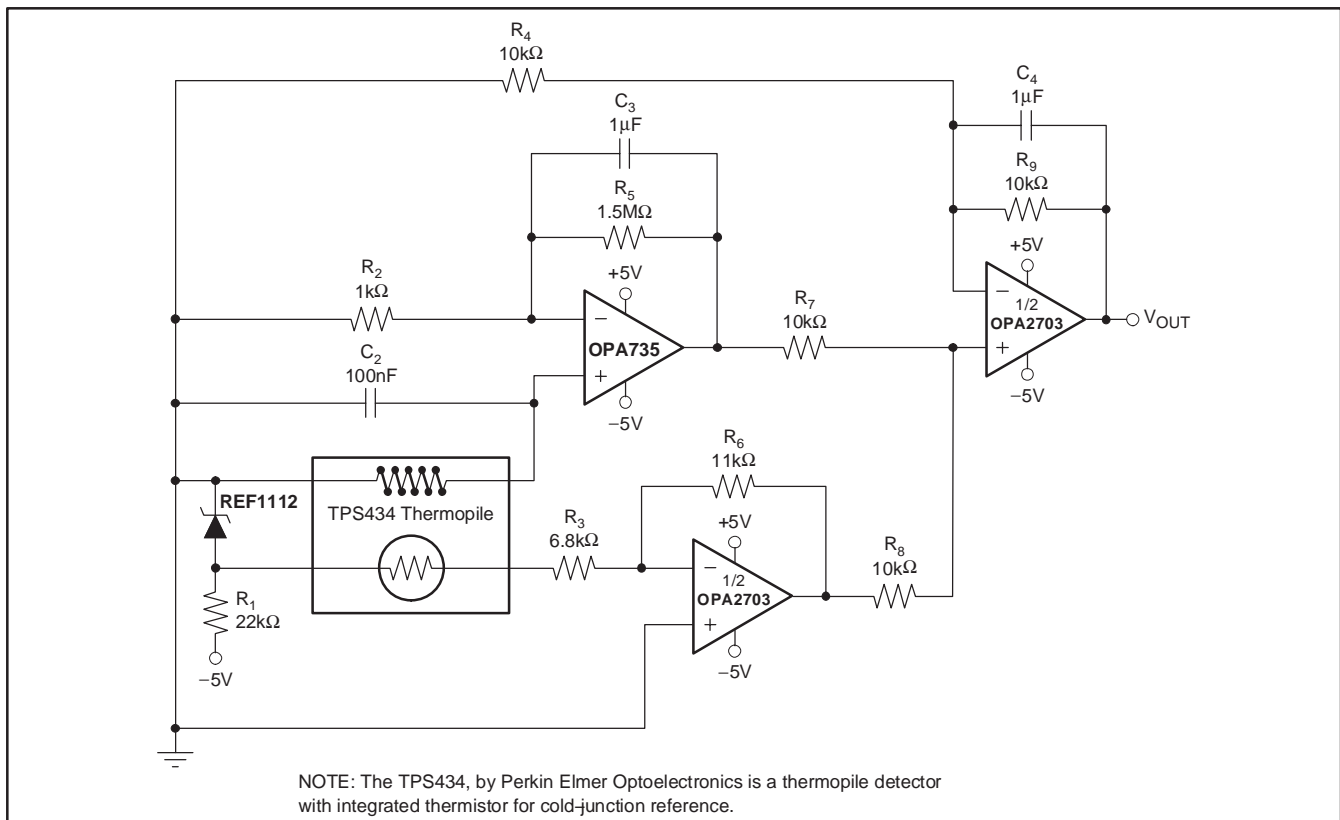


Figure 5. Thermopile Non-Contact Surface Temperature Measurement

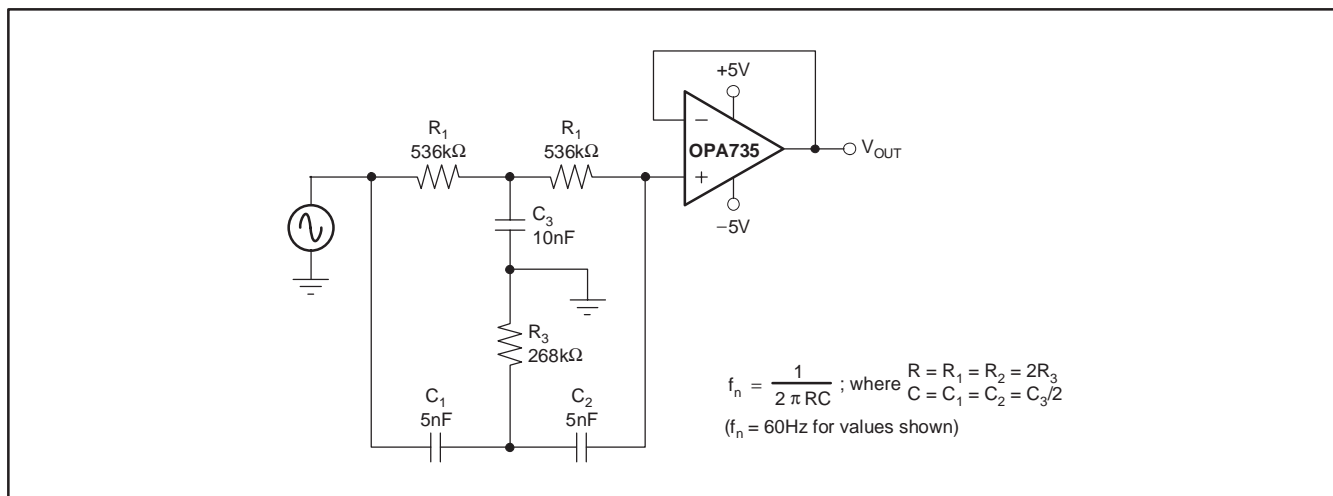


Figure 6. Twin-T Notch Filter

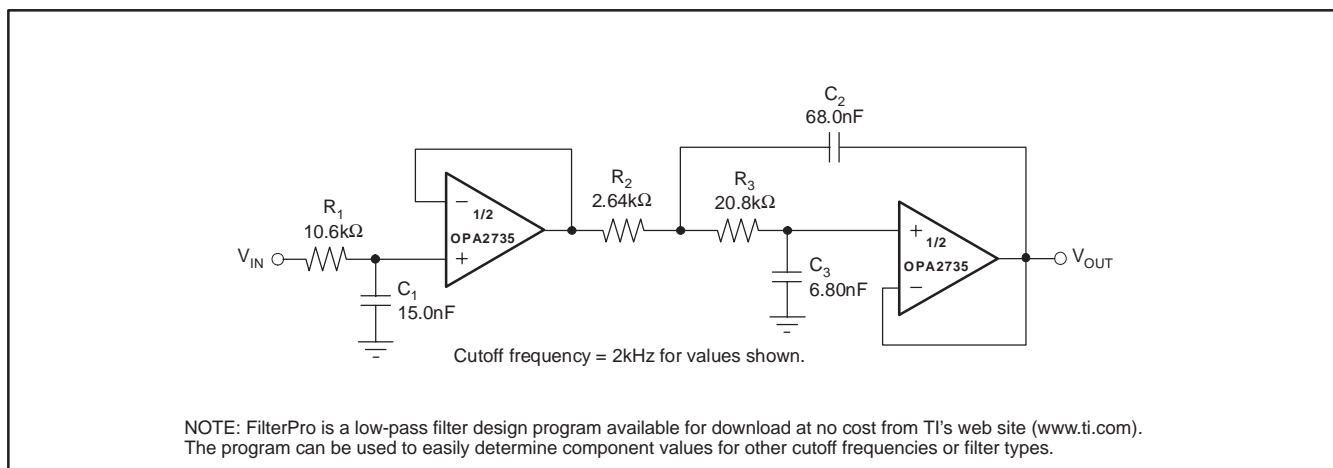


Figure 7. High DC Accuracy, 3-Pole Low-Pass Filter

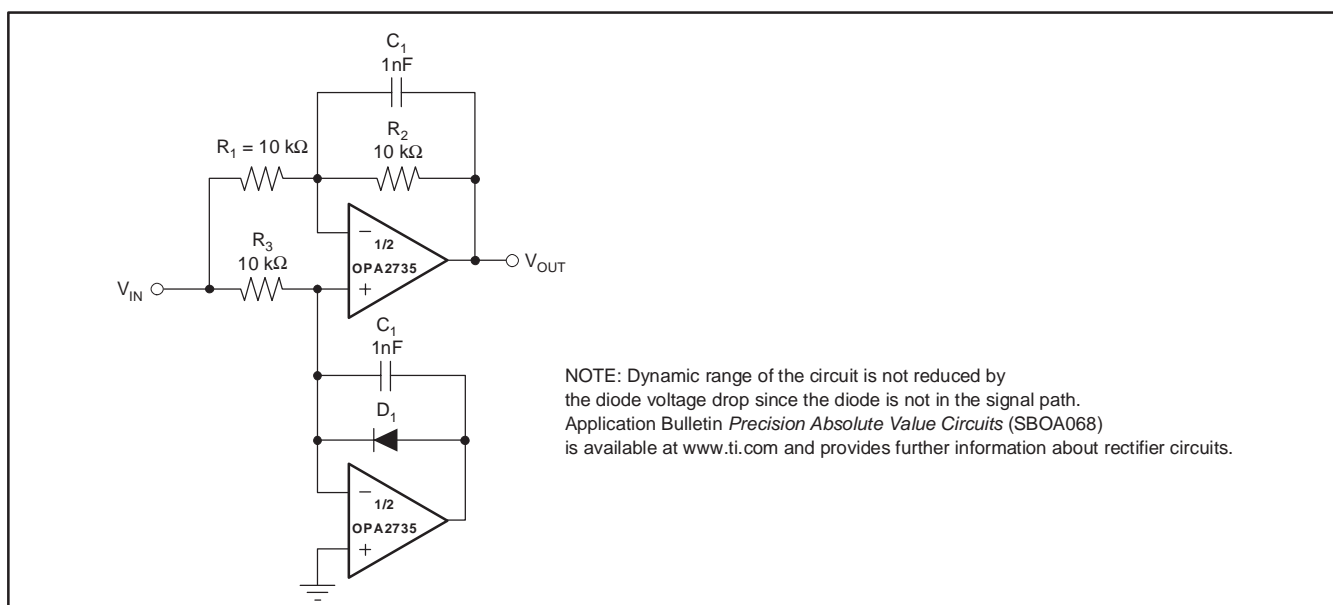
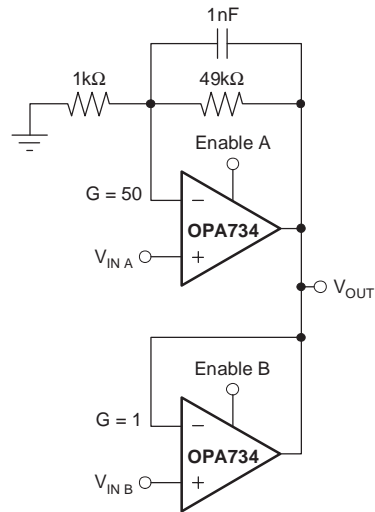


Figure 8. Precision Full-Wave Rectifier with Full Dynamic Range



Enable inputs are CMOS logic compatible.

Figure 9. High-Precision 2-Input MUX for Programmable Gain

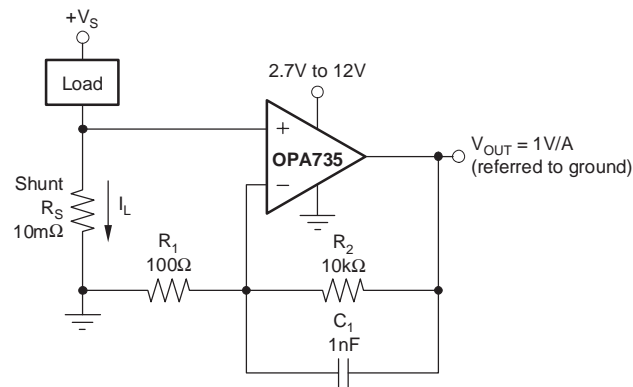
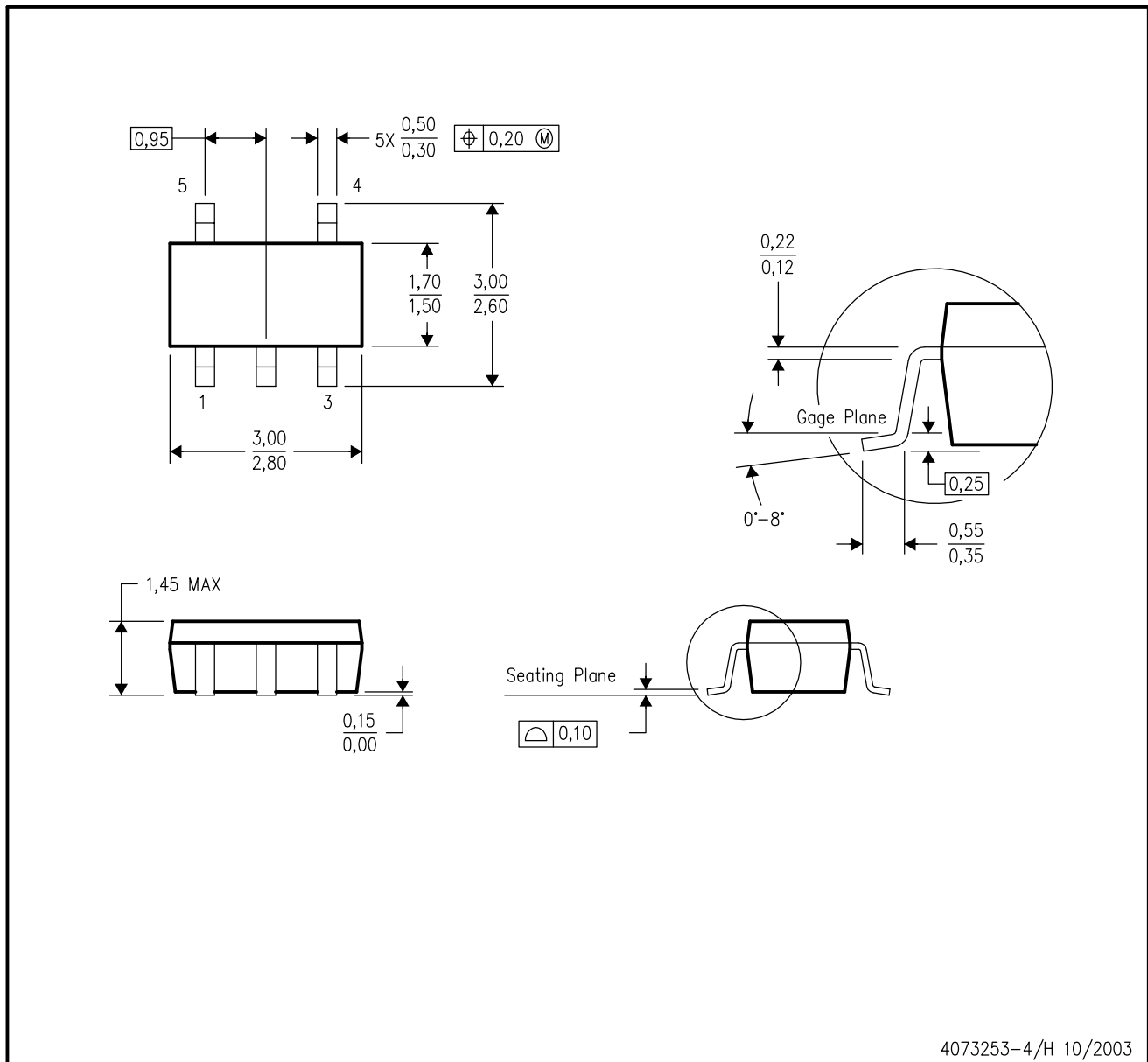


Figure 10. Low-Side Power-Supply Current Sensing

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

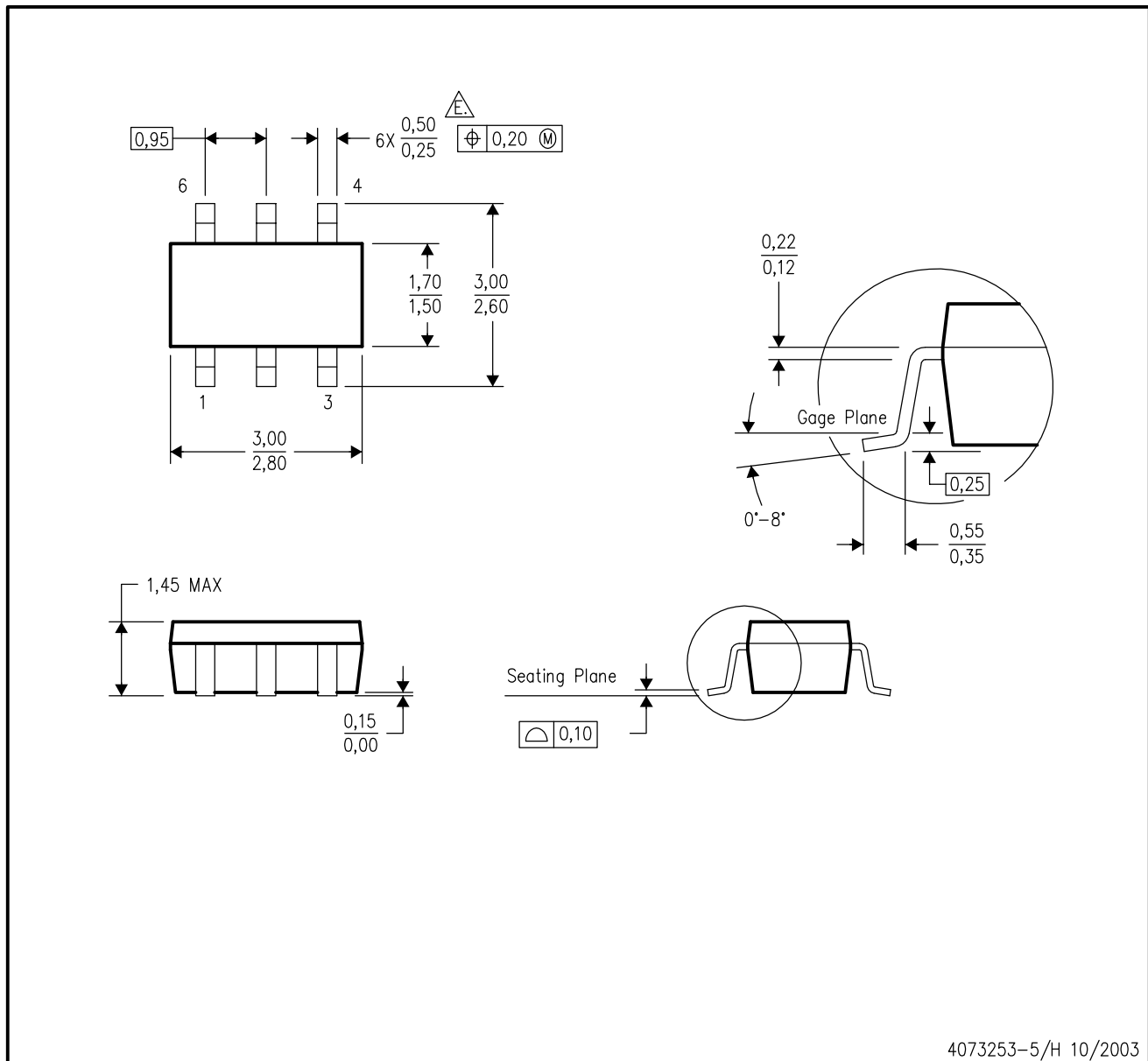


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- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G6)

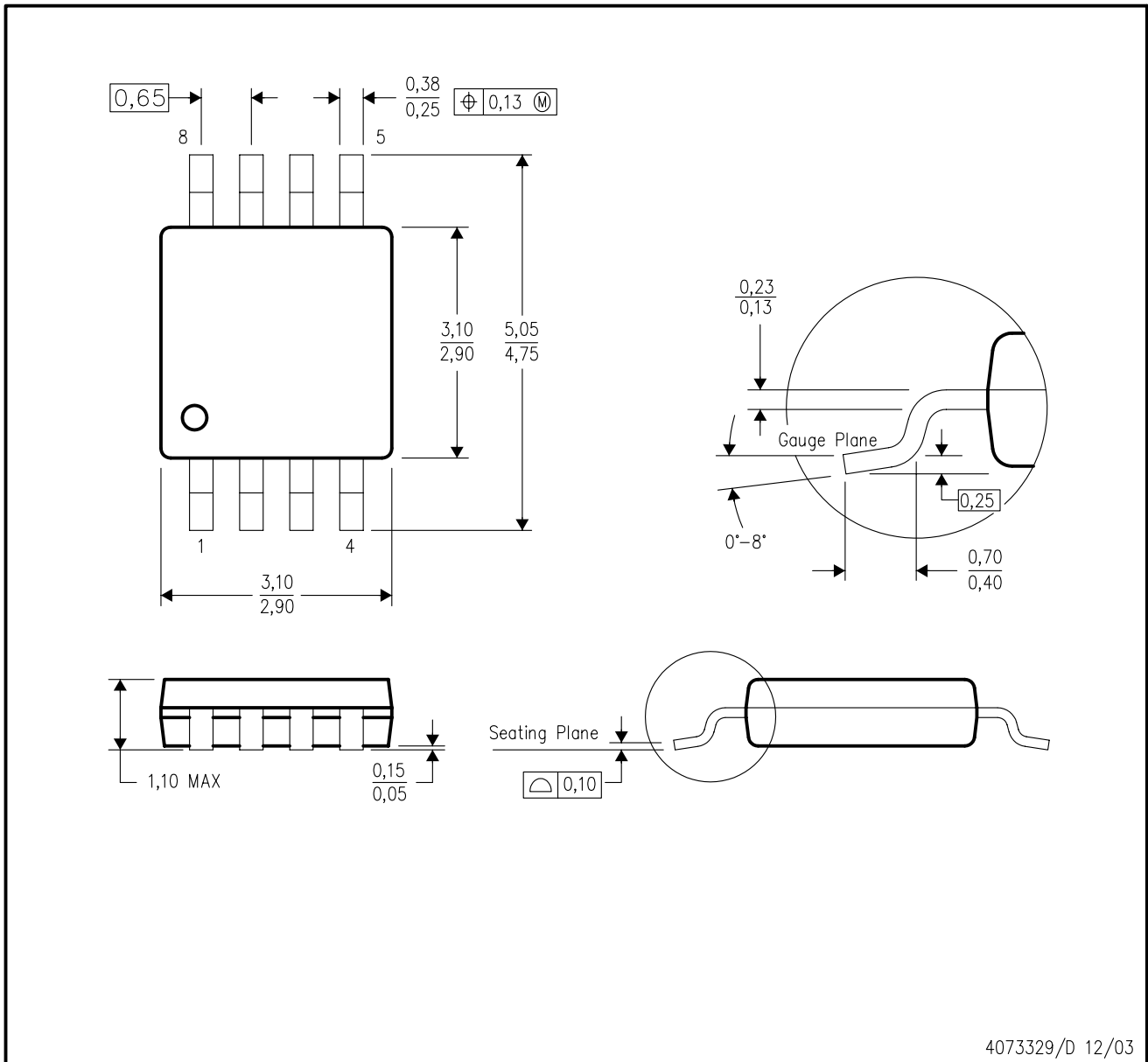
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- Δ Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DGK (S-PDSO-G8)

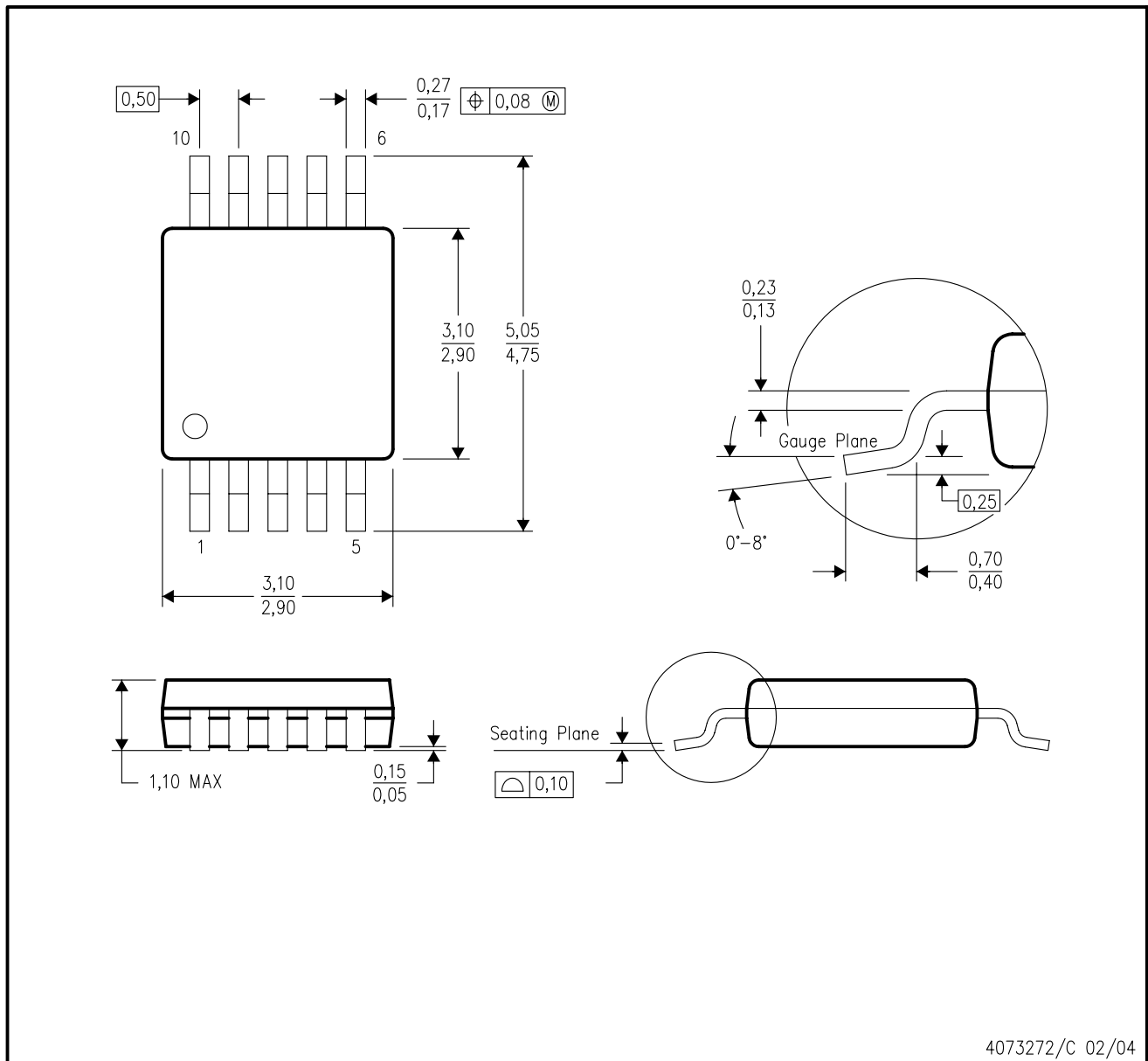
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation AA.

DGS (S-PDSO-G10)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

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