KA7632/KA7633

Fixed Multi-output Regulator

Features

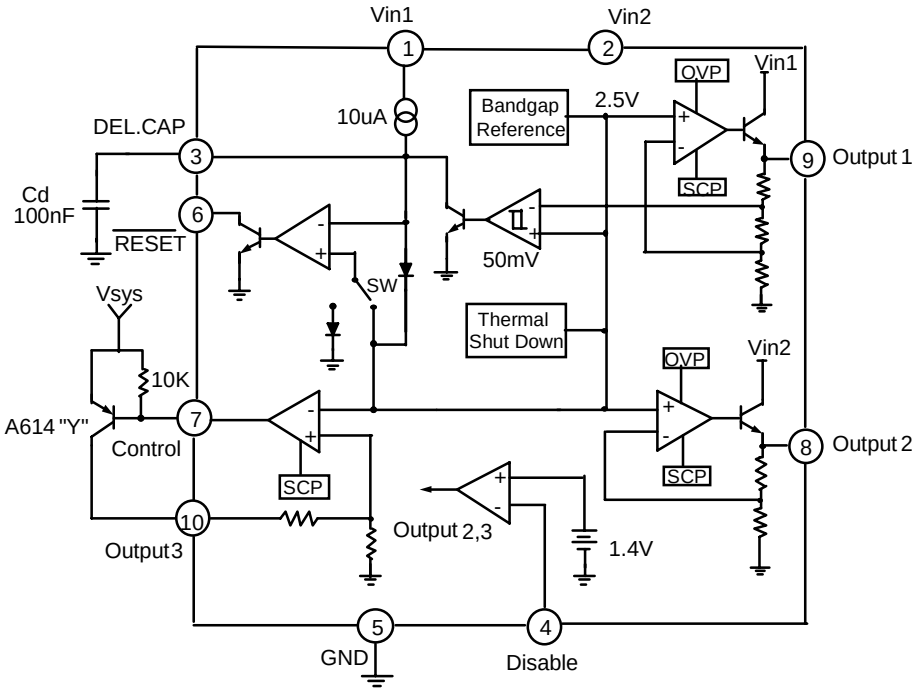
- Output Currents up to 0.5A (output1 & 2)
- Output Current up to 1A with External Transistor (output3)
- Fixed Precision Output 1 voltage 3.3V ± 2%
- Fixed Precision Output 2 voltage 8V ± 2% (KA7632)
- Fixed Precision Output 2 voltage 9V ± 2% (KA7633)
- Control Signal Generator for Output 3 voltage (5.1V ± 2%)
- Reset Facility for Output Voltage1
- Output 2,3 with Disable by TTL Input
- Current Limit Protection at Each Output
- Thermal Shut Down

Description

The KA7632/KA7633 is a multi-output positive voltage regulator designed to provide fixed precision output voltages of 3.3V, 8V (KA7632) / 9V (KA7633) at current up to 0.5A and 5.1V at current up to 1A with external PNP transistor. An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated value. Output2 & 3 can be disabled by TTL input. Protection features include over voltage protection, short circuit protection and thermal shutdown.

10-SIP H/S

Internal Block Diagram



Rev. 1.0.1

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Remark
DC Input Voltage	Vin	20	V	-
Disable Input Voltage	Vc	20	V	-
Output Current	Io	0.5	A	-
Power Dissipation	Pd	1.5	W	No Heatsink
Junction Temperature	Tj	+150	°C	-
Operating Temperature	Topr	0~+125	°C	-

Electrical Characteristics(KA7632)

(Refer to test circuit Vin1=6V ,Vin2=10.5V ,Tj = +25 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage 1	Vo1	Io1=10mA 6V<Vin1<14V 5mA<Io1<500mA	3.22 3.14	3.3 3.3	3.38 3.46	V
Output Voltage 2	Vo2	Io2=10mA 10.5V<Vin2<18V 5mA<Io2<500mA	7.84 7.7	8 8	8.16 8.3	V
Dropout Output Voltage 1,2	Vd1,2	Io1,2=500mA	-	-	2.5	V
Line Regulation 1,2	ΔVo 1,2	6V <Vin1<14V 10.5V <Vin2<18V Io1,2 = 200mA	-	-	40 80	mV
Load Regulation 1,2	ΔVo 1,2	5mA < Io1< 500mA 5mA <Io2< 500mA	-	-	70 160	mV
Output Voltage 3	Vo3	Vsys=7V, Io3=100mA	4.97	5.1	5.23	V
Line Regulation 3	ΔVo3	13V< Vin2 <18V, Io3 =100mA	-	-	50	mV
Load Regulation 3	ΔVo3	5mA < Io3 < 1A	-	-	110	mV
Reset Pulse Delay	Trd	Cd=100nF, Note1	-	25	-	ms
Saturation Voltage in Reset Condition	VrL	I6=5mA	-	-	0.4	V
Leakage Current at Pin 6	IrH	V6=10V	-	-	10	μA
Output Voltage Thermal Drift	STt	0 °C <Tj < +125 °C , Note 2	-	100	-	ppm/°C
Short Circuit Output Current	Isc1,2	Vin1=6V ,Vin2 =10.5V	-	-	1.6	A
Disable Voltage High	VdisH	Output 2 Active	2	-		V
Disable Voltage Low	VdisL	Output 2 Disabled	-	-	0.8	V
Disable Bias Current	Idis	0V < Vdis < 7V	-100	-	2	μA
Junction Temperature for TSD	Ttsd	Note 2	-	145	-	°C
Quiescent Current	Iq	Io1=10mA, Output2 Disabled	-	-	2	mA
Reset Threshold Voltage	Vr	K=Vo1	K-0.4	K-0.25	K-0.1	V
Reset Threshold Hysteresis	Vrth	Note 1	20	50	100	mA

Notes:

1. To check the reset circuit ,the reset output is low to discharge the delay capacitor(=Cd). if it's less than Vo1-0.25V. And the reset output is high when the delay capacitor voltage linearly increased by the interal current source(10μA) if it's more than Vo1- 0.2V. The equations of delay time is same as below. Trd = (Cd × 2.5) / 10μA
2. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics(KA7633)

(Refer to test circuit Vin1=6V ,Vin2=11.5V ,Tj = +25 °C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage 1	Vo1	Io1=10mA 6V<Vin1<14V 5mA<Io1<500mA	3.22 3.14	3.3 3.3	3.38 3.46	V
Output Voltage 2	Vo2	Io2=10mA 11.5V<Vin2<18V 5mA<Io2<500mA	8.82 8.65	9 9	9.18 9.35	V
Dropout Output Voltage 1,2	Vd1,2	Io1,2=500mA	-	-	2.5	V
Line Regulation 1,2	ΔVo 1,2	6V <Vin1<14V 11.5V <Vin2<18V Io1,2 = 200mA	-	-	40 80	mV
Load Regulation 1,2	ΔVo 1,2	5mA < Io1< 500mA 5mA <Io2< 500mA	-	-	70 160	mV
Output Voltage 3	Vo3	Vsys=7V, Io3=100mA	4.97	5.1	5.23	V
Line Regulation 3	ΔVo3	13V< Vin2 <18V, Io3 =100mA	-	-	50	mV
Load Regulation 3	ΔVo3	5mA < Io3 < 1A	-	-	110	mV
Reset Pulse Delay	Trd	Cd=100nF, Note1	-	25	-	ms
Saturation Voltage in Reset Condition	VrL	I6=5mA	-	-	0.4	V
Leakage Current at Pin 6	IrH	V6=10V	-	-	10	μA
Output Voltage Thermal Drift	STt	0 °C <Tj < +125 °C , Note 2	-	100	-	ppm/°C
Short Circuit Output Current	Isc1,2	Vin1=6V ,Vin2 =11.5V	-	-	1.6	A
Disable Voltage High	VdisH	Output 2 Active	2	-		V
Disable Voltage Low	VdisL	Output 2 Disabled	-	-	0.8	V
Disable Bias Current	Idis	0V < Vdis < 7V	-100	-	2	μA
Junction Temperature for TSD	Ttsd	Note 2	-	145	-	°C
Quiescent Current	Iq	Io1=10mA, Output2 Disabled	-	-	2	mA
Reset Threshold Voltage	Vr	K=Vo1	K-0.4	K-0.25	K-0.1	V
Reset Threshold Hysteresis	Vrth	Note 1	20	50	100	mA

Notes:

1. To check the reset circuit ,the reset output is low to discharge the delay capacitor(=Cd). if it's less than Vo1-0.25V. And the reset output is high when the delay capacitor voltage linearly increased by the interal current source(10μA) if it's more than Vo1- 0.2V. The equations of delay time is same as below. Trd = (Cd × 2.5) / 10μA
2. These parameters, although guaranteed, are not 100% tested in production.

Typical Perfomance Characteristics

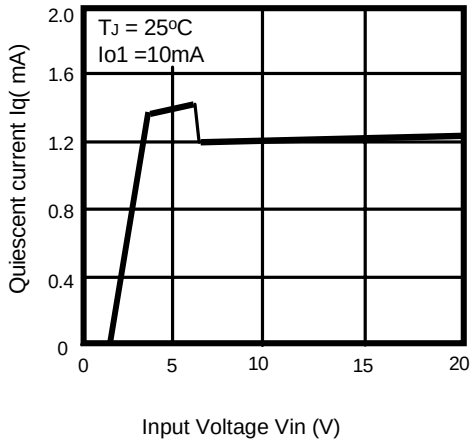


Figure 1. Quiescent Current vs. Input Voltage

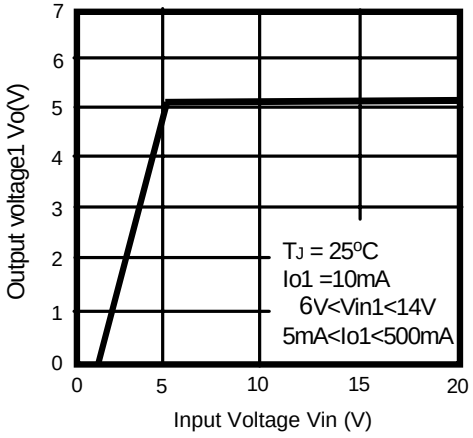


Figure 2. Output Voltage1 vs. Input Voltage

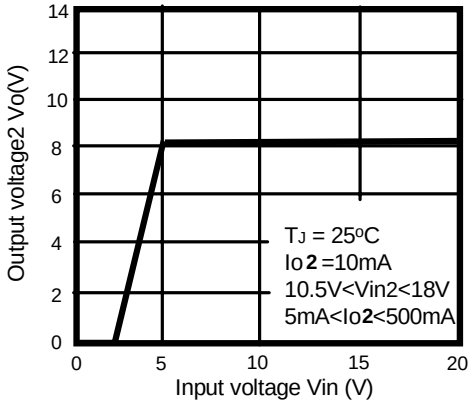


Figure 3. Output Voltage2 vs. Input Voltage

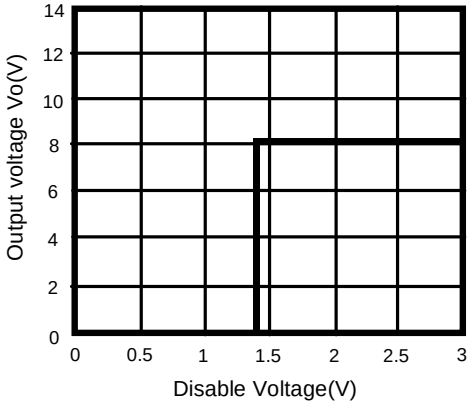


Figure 4. Output Voltage vs. Disable Voltage High(Low)

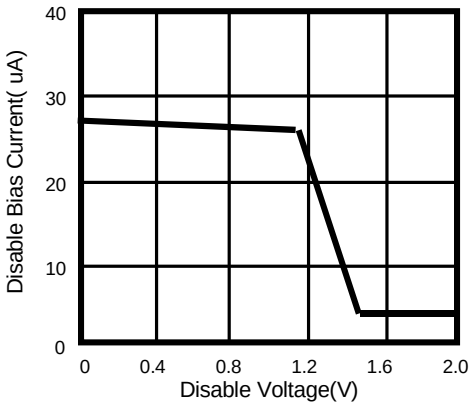


Figure 5. Disable Bias Current vs. Disable Voltage

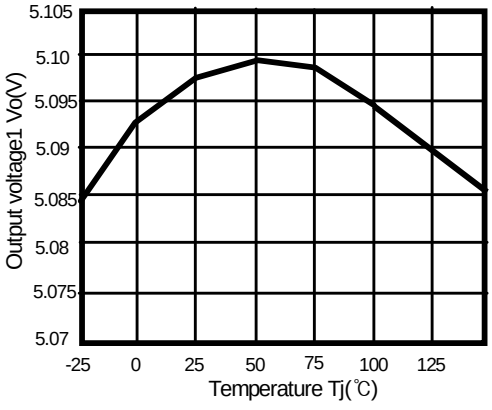


Figure 6. Output Voltage1 vs. Temperature(Tj)

Typical Perfomance Characteristics (continued)

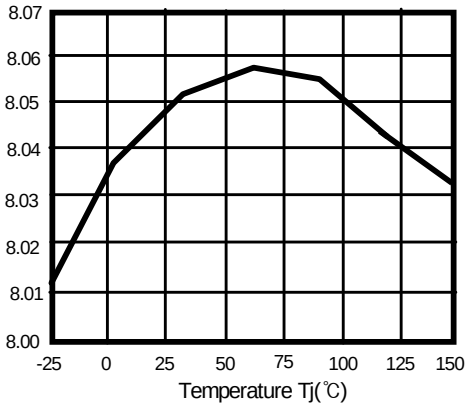


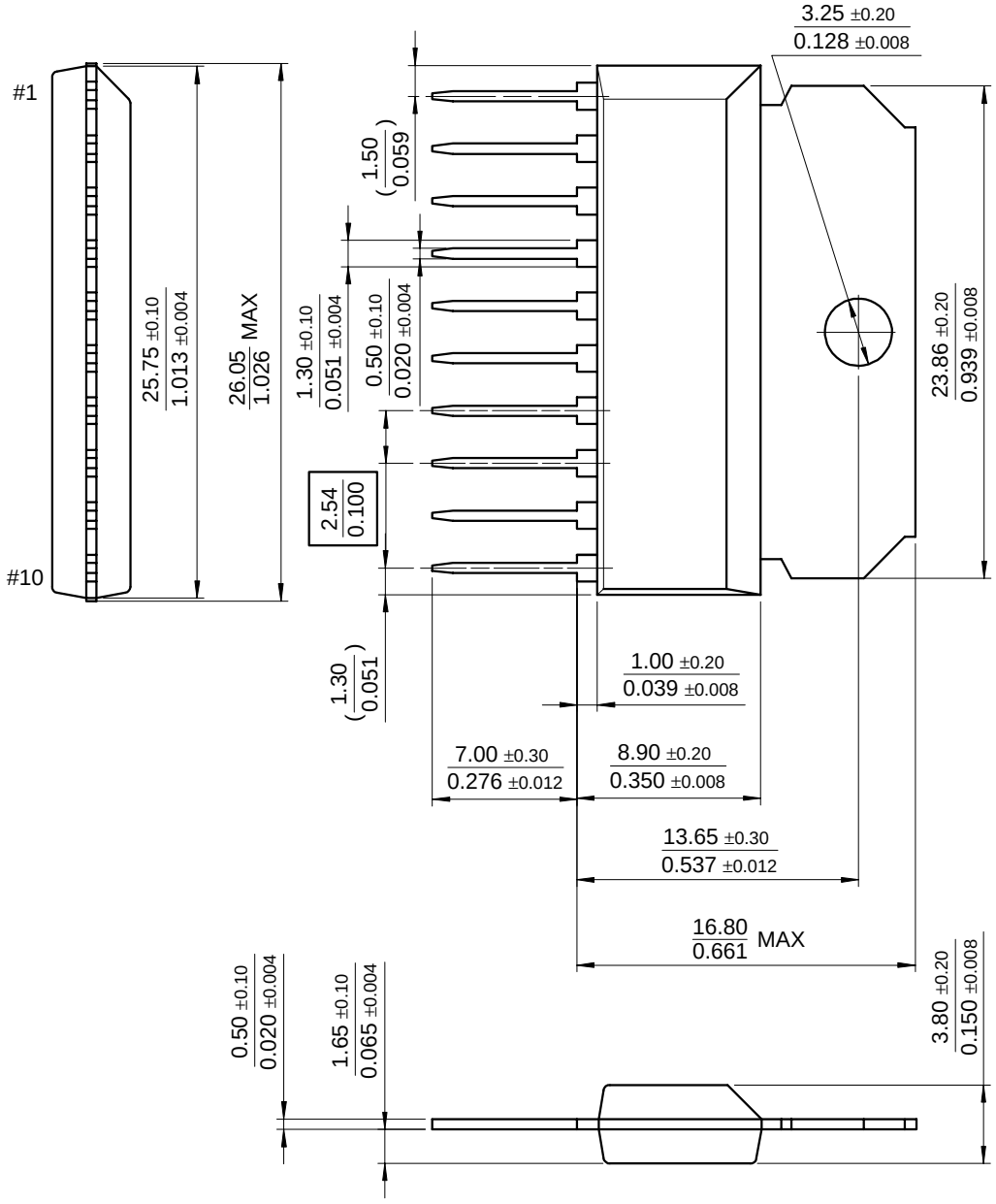
Figure 7. Output Voltage2 vs. Temperature(Tj)

Mechanical Dimensions

Package

Dimensions in millimeters

10-SIP H/S



Ordering Information

Product Number	Package	Operating Temperature
KA7632	10-SIP H/S	0°C to +125°C
KA7633		